A CMOS FTFN Realization with Constant-g_m Rail-to-Rail Input Stage

Mustafa Saygıner, Mustafa Altun, and Hakan Kuntman

***Abstract*-- In this paper, an alternative CMOS realization of an FTFN with a rail-to-rail input stage is proposed. Input stage of the presented circuit is based on a three-times current mirror to realize lowered *gm* deviation within the whole common-mode input range. Output stage of the FTFN is constructed with using active-feedback cascode current mirrors to obtain higher output resistance at the output nodes *Z* and *W*. The performance of the proposed FTFN structure is simulated with a novel grounded inductance simulating topology with applying on a third-order high-pass filter. All simulation results are given using SPICE simulation program.**

***Index Terms*-- Active Network Synthesis, CMOS FTFN, Inductance Simulating.**

I. INTRODUCTION

A Four Terminal Floating Nullor (FTFN) is equivalent to an ideal nullor or is called operational floating amplifier [1]. Using nullor concept with the four floating terminals brings out some advantageous in the active network synthesis. For instance, by using adjoint network concept, voltage mode topologies can be transformed efficiently into their currentmode counterparts or vice versa by using nullor concept – so that by using FTFNs [2, 3]. There are some methods proposed to implement FTFNs. Supply current sensing method (SCSM) and using two commercial current-feedback operational amplifiers are the most well-known FTFN implementations [4]. By the way, in the literature, there can be observed many attempts for realizing CMOS FTFNs to implement currentmode applications. Çam and Kuntman implemented two CMOS version of FTFN with a maximum transconductance gain of 160mA/V [5, 6]. Jiraseree-amornkun and Surakampontorn also implemented a constant-g_m rail-to-rail FTFN with a transconductance gain of 120mA/V [7]. There is also a very high transconductance gain CMOS FTFN realization with a gain of 3000A/V has been implemented by Saygıner and Kuntman with relativly low bandwidth [8, 11].

In this study, a new CMOS FTFN implementation with a lowered g_m deviation with the rail-to-rail input is proposed. The transconductance gain of the proposed structure is about 370mA/V and 3dB cut-off frequency of the gain can be estimated as 1.8MHz. Overall performance of the proposed FTFN is observed by using SPICE program and a novel grounded inductance simulating topology which employes two FTFNs is proposed to show performance of the CMOS FTFN.

M. Saygıner is with Istanbul Technical University Department of Electronics and Communication Engineering, 34469 Maslak, Istanbul, Turkey (e-mail: sayginer@itu.edu.tr)

M. Altun is with University of Minnesota, Minneapolis, USA (e-mail: altunmus@itu.edu.tr)

H. Kuntman is with the Istanbul Technical University Department of Electronics and Communication Engineering, 34469 Maslak, (e-mail: kuntman@itu.edu.tr)

II. CIRCUIT DESCRIPTION

The symbolic port relation of the FTFN is shown in Fig. 1a and the nullor model of the ideal FTFN is shown in Fig. 1b. An FTFN can be characterized as follows,

$$\begin{aligned} v_X &= v_Y \\ i_Z &= i_W \\ i_X &= i_Y = 0 \end{aligned} \tag{1}$$

By the definition of the nullor, nullator section of the nullor model has arbitrary terminal impedances. In the FTFN realization, generally the output *Z* and *W* terminal impedances are chosen as high impedances.

A. CMOS FTFN Input Stage

To construct a constant-*gm* rail-to-rail input stage, Fig. 2 implementation of the input stage is obtained. To increase the common-mode input voltage range, the N-channel input pair, M1-M4, and the P-channel input pair, M2-M3 are placed in parallel. By this way, at high common-mode voltage ranges only N-channel input pair operates. On the other hand, with the low common-mode voltage range only P-channel input pair operates. With the intermediate common-mode voltages, both P and Nchannel input pairs operate [9].

Since there are three regions of operation for the input stage, there are three different regions for the total input transconductance, g_{mT} which can be expressed as

$$\begin{aligned} g_{mT} &= g_{mN} + g_{mP} \\ g_{mT} &= \sqrt{K_N I_N} + \sqrt{K_P I_P} \end{aligned} \tag{2}$$

where K is defined as,

$$K = \mu C_{ox} \frac{W}{L} \tag{3}$$

and I_N , I_P are the tail currents of the N and P-channel input pairs respectively.

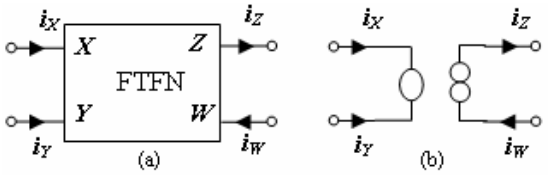

Fig. 1. a) FTFN Symbol. b) Nullor equivalent.

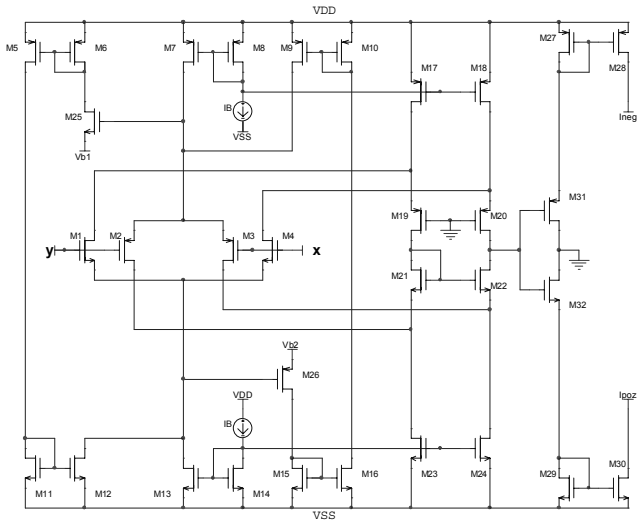

Fig. 2. Input stage of the proposed FTFN.

When only one input pair operates, in order to have a constant g_{mT} value at the input stage, the tail current of the actual active input pair has to be increased. Since the g_m of an input pair is proportional to the square root of its tail current, the tail current of the actual active input pair has to be increased by a factor of 4 [9]. To make this implementation, M5, M6, M11, M12 and M25 transistors are used for the N-channel pair and M9, M10, M15, M16 and M26 is used for the P-channel pair. The current mirroring ratio between the transistors M11-M12 and M9-M10 is equal to 1:3. M17-M24 transistors are used for current summation at the output of the input stage.

Fig 3. shows the simulation result of g_{mT} versus input common mode change with the transistors dimensions given in Table I.

It can be observed from Fig. 3 that the g_{mT} value is changing only maximum +25% around specific ±0.75V input common-mode values.

Transistors M31 and M32 are two common drain stages to achieve high current gain from the voltage gain exist at the high impedance nodes-drain nodes of M20 and M21.

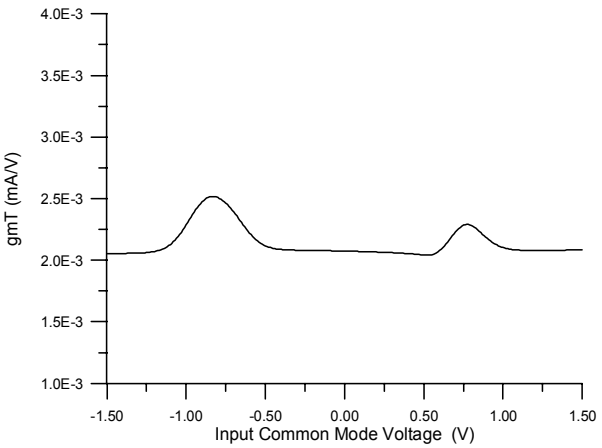

Fig. 3. g_{mT} vs. Input common-mode voltage

TABLE I. TRANSISTOR DIMENSIONS OF THE INPUT STAGE.

Transistor Name	Width [µm]	Length [µm]
M1, M4, M5-M8, M10, M12, M21-M24, M32	45	0.7
M2,M3, M31	120	0.7
M17-M20	100	0.7
M11, M13-M16	15	0.7
M9	135	0.7
M25, M26	50	0.7
M27	100	1.4
M28	150	1.4
M29	30	1.4
M30	45	1.4

B. *Designing the Output Stage*

FTFN outputs Z and W in fact have arbitrary impedances and for a $I_Z=I_W$ current relation, high output impedances are prefered here to be implemented.

Output stage of the FTFN is constructed with using active-feedback cascode current mirrors [10] to get high output impedance at the output nodes Z and W.

Completed output stage design is seen in Fig. 5. Transistor dimensions of the stage is given in Table II.

TABLE II. TRANSISTOR DIMENSIONS OF THE OUTPUT STAGE.

Transistor Name	Width [µm]	Length [µm]
All N-Channel Transistors	45	0.7
All P-Channel Transistors	15	0.7

Simulated output impedances of the proposed FTFN is shown in Fig. 4. It can be shown that the output impedances of the Z and W terminals are about 1.2GΩ.

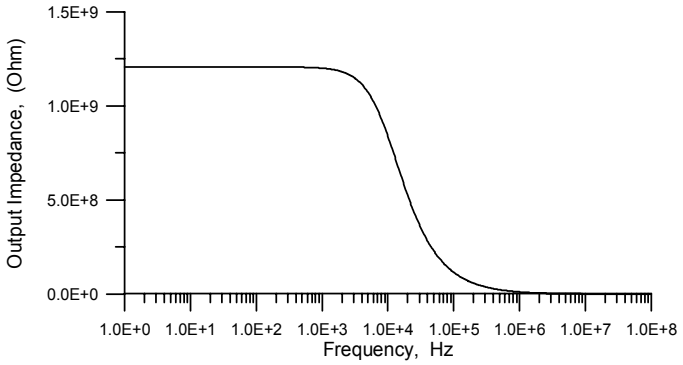

Fig. 4. Output impedance of the proposed FTFN.

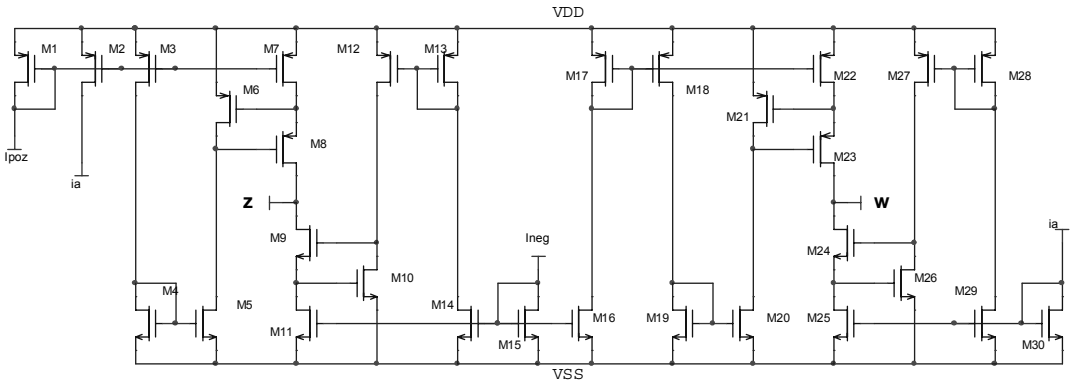

Fig. 5. Output stage of the proposed CMOS FTFN

C. *Performance of the Proposed FTFN*

The performance of the proposed CMOS rail-to-rail input stage FTFN is simulated with using SPICE simulation program. For the transistor models, AMS 0.35µm BSIM 3v3 parameter set is used. The most important performance parameter of the FTFN is the transconductance gain over the whole frequency. By simulating the proposed CMOS FTFN, transconductance gain can be given like in Fig. 6. It can be seen that the transconductance gain is about 370 mA/V with a cut-off frequency of 1.8MHz.

Table III. is given to summarize performance of the proposed FTFN.

TABLE III. PERFORMANCE SUMMARY OF THE PROPOSED FTFN.

Parameter	*Simulation Results*
Supply Voltages	±1.5V
g_{mT}	2.015 mA/V (Δg_{mT}= +0.55 mA/V)
Biasing Voltages	V_{b1}=0.4V V_{b2}= -0.5V
Biasing Currents	I_B=100µA
Input Off-set Voltage	1.14mV
Power Dissipation	4.44mW
Transconductance Gain	370 mA/V
Cut-off Frequency	1.8 MHz
Output Current Swing	±1.25mA
Output Impedances (*Z, W*)	1.2GΩ

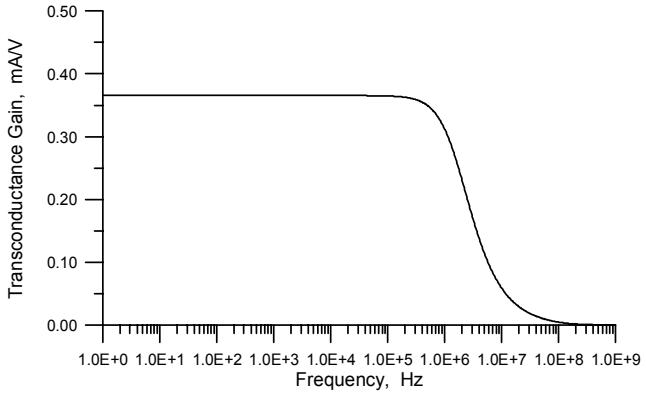

Fig. 6. Transconductance of the proposed FTFN.

III. APPLICATION OF THE FTFN

Proposed CMOS FTFN is tested in a novel grounded inductance simulating circuit shown in Fig. 7. Proposed topology is consisted of two FTFNs, four resistors and a capacitor.

By taking the simple nodal analysis, it can be shown that the impedance equation can be written as,

$$Z(s)=\frac{v}{i}=sL_{eq}=s\frac{R_1R_2R_4}{R_3}C \tag{4}$$

Therefore, the simulated inductance can be re-written as,

$$L_{eq}=\frac{R_1R_2R_4}{R_3}C \tag{5}$$

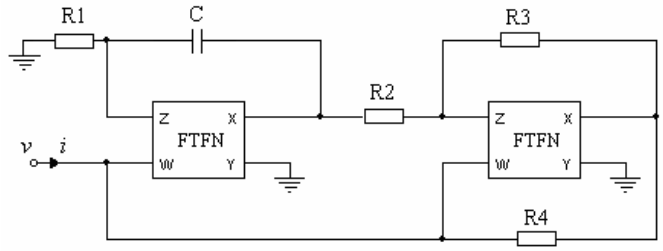

Fig. 7. Grounded inductance simulating using FTFNs.

A maximally flat-band third-order high-pass filter with a 50Ω input/output impedances can be constructed using passive LC elements as shown in Fig 8.

By choosing 1MHz cut-off frequency, passive elements can be calculated from ANSOFT Filter Design Program as C_1=C_2=C=3.18nF, L=3.98µH and R_S=R_{Load}=R=50Ω. Then filter transfer function can be written as,

$$\frac{v_0}{v_i}(s)=\frac{RLC^2s^3}{2RLC^2s^3+(R^2C^2+2LC)s^2+2RCs+1} \tag{6}$$

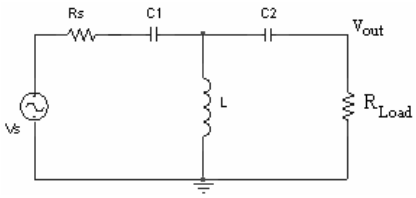

Fig. 8. A passive implementation of third-order high-pass filter.

By using the proposed grounded inductance simulation, above passive filter can be implemented with using FTFNs. Passive element values for the inductance simulating are chosen as $R_1=R_2=1k\Omega$, $R_4=10k\Omega$, $R_3=100k\Omega$ and C=39.7pF. Simulated filter characteristics can be shown with the ideal behaviour in Fig. 9. It can be observed from Fig. 9 that the simulation result and the ideal case are agreed well in together.

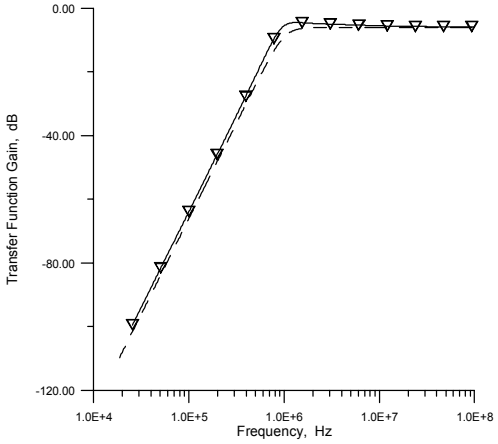

Fig. 9. Third-order high-pass filter characteristics where the dashed-line is showing the ideal case.

To investigate the large-signal behaviour of the filter, a 1MHz rail-to-rail input sinusoidal with a 1.5V peak-to-peak amplitude is applied and the total harmonic distortion at the output observed around 1.75%.

IV. Conclusion

In this study, an alternative CMOS realization of FTFN with a rail-to-rail input stage is proposed. Performance of the proposed FTFN is simulated with SPICE simulation program. For the application of the FTFN, a novel grounded inductance circuit using two FTFNs is proposed. A third-order high-pass filter is used to observe inductance performance. All simulations show that the proposed CMOS FTFN can be used as an alternative structure.

V. References

[1] J. H. Huijsing, "Operational floating amplifier (OFA)." In IEE Proc. 137(2), part G, pp. 131–136, 1990.

[2] W. S. Director and R. A. Rohrer, "Automated Network Design- The Frequency Domain Case", IEEE Trans. on Circuit Theory, CT-16, no 3, pp. 330-337. August, 1969.

[3] G. W. Roberts, A. S. Sedra, "A General Class of Current Amplifier-Based Biquadratic Filter Circuits" IEEE Transaction on Circuit and Systems-I: Fundamental Theory and Applications, 39, 257-263, 1992.

[4] W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "A realization of current-mode biquadratic filters using multiple-output FTFNs," Proceeding of IEEE APCCAS2000, pages 201-204, 2000.

[5] U. Çam, H.Kuntman, CMOS four terminal floating nullor (FTFN) design using a simple approach, Microelectronics Journal, Vol.30, No. 12, pp.1187-1194, 1999.

[6] U. Çam and H. Kuntman, "A new CMOS realisation of four terminal floating nullor (FTFN)", International Journal of Electronics, Vol. 87, No.7, pp 809-817, 2000.

[7] A. Jiraseree-Amornkun and W. Surakampontorn, "Constant-g_m Rail-to – Rail CMOS Multi-Output FTFN" The 2002 International Technical Conference On Circuits/Systems, Computers and Communications,

Phuket, Thailand, pp.333-336, July 2002.

[8] M. Saygıner, H. Kuntman, "Yüksek geçiş iletkenli yeni bir CMOS FTFN gerçeklemesi", ELECO'06, Proc. of Nat.. Conference on Electrical and Electronics Eng., Electronics:, pp.50-55, Bursa, 2006.

[9] R. Hogervorst, R.J. Wiegerink, P.A. de Jong, J. Fonderie, R.F. Wassenaar, and J.H. Huijsing, "CMOS low-voltage operational amplifiers with constant-g_m rail-to-rail input stage" Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 2876-2879, 1992.

[10] A. Zeki and H. Kuntman: Accurate active-feedback CMOS cascode current mirror with improved output swing, International Journal of Electronics, Vol.84, No.4, pp.335-343, 1998.

[11] M. Saygıner, H. Kuntman, "Realization of First-Order All-Pass Filter Using Four Terminal Floating Nullor", Proceedings of Applied Electronics 2006,pp. 159-161, Pilsen, Czech Republic, 6-7 September 2006.

[12] M. Saygıner, "Yeni FTFN yapıları ve uygulamaları", M.Sc. Thesis, Istanbul Technical University, Institute of Science and Technology, 2007.

VI. Biographies

Mustafa Saygıner received the B.Sc. and M.Sc.degrees from IstanbulTechnical University, Istanbul, Turkey, in 2004 and 2007, respectively. He is currently a Ph.D. student in ITU and workingas a Research & Teaching Asistant in the Electronics and Communication Engineering Department of Istanbul Technical University. His research interest include Analog IC design and RF circuit design.

Mustafa Altun received the B.Sc. and M.Sc. degrees from Istanbul Technical University, Istanbul, Turkey, in 2004 and 2007, respectively. He is currently a Ph.D. student in the University of Minnesota, Minneapolis, USA. He is also a Research & Teaching Asistant in the Electronics and Communication Engineering Department of Istanbul Technical University. His research interest include Analog and Digital IC design, VLSI Systems.

H. Hakan Kuntman received the B.Sc., M.Sc., and Ph.D. degrees from Istanbul Technical University (ITU), Istanbul, Turkey, in 1974, 1977, and 1982, respectively. In 1974, he joined the Electronics and Communication Engineering Department of ITU. Since 1993, he has been a Professor of Electronics in the same department. His research interest include design of electronic circuits, modeling of electron devices and electronic systems, active filters, design of analog IC topologies. He has authored many publications on modeling and simulation of electron devices and electronic circuits for computer-aided design, analog VLSI design, and active circuit design. He is the author or the coauthor of 82 journal papers published or accepted for publishing in international journals, 104 conference papers presented or accepted for presentation in international conferences, 112 turkish conference papers presented in national conferences and ten books related to the above mentioned areas.