Noise-induced Performance Enhancement of Variability-aware Memristor Networks

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***Abstract*—Memristor networks are capable of low-power, massive parallel processing and information storage. Moreover, they have widely used for a vast number of intelligent data analysis applications targeting mobile edge devices and low power computing. However, till today, one of the major drawbacks resulting to their commercial cumbersome growth, is the fact that the fabricated memristor devices are subject to device-to-device and cycle-to-cycle variability that strongly affects the performance of the memristive network and restricts, in a sense, the utilisation of such systems for real-life demanding applications. In this work, we put effort on increasing the performance of memristive networks by incorporating external additive noise that will be proven to have a beneficial role for the memristor devices and networks. More specifically, we are taking inspiration from the well-known non-linear system phenomenon, called Stochastic Resonance, which alleges that noisy signals with specific characteristics can positively affect the operation of non-linear devices. As such, we are now focusing on the utilisation of the phenomenon on memristor devices in a way that the negative effect of variability is reduced, thus the operation of the whole memristor network is assisted by the increased variability tolerance. The presented results of Bit Error Rate (BER) on a small ReRAM crossbar array sound promising and enable us to further investigate the exploitation of the described phenomenon by memristor-based networks and memories.**

I. Introduction

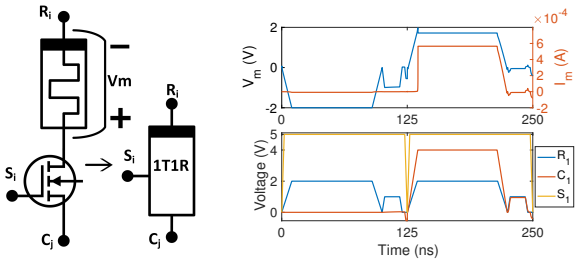
Conventional CMOS-based computers have almost reached their maximum capabilities for consumer products, but the needs for memory and storage are continuously increasing. As a result, novel memory and computing technologies are developed to tackle with the memory wall problem and scale up further the performance of the computing systems. Out of the research for novel electronics, memristor devices and networks reached the spotlight of emerging technologies [1].

Memristor networks provide an emergent tool for information storage and processing in the same physical place [2], realizing efficient in-memory computing for real-time, power-efficient and high-performance applications. One of the biggest obstacles towards the use of memristor networks in actual commercial products is the variability of the manufactured memristor devices, where either cycle-to-cycle (temporal) or device-to-device (spatial) variations are evident and restrict the robustness of the memristor network as a system [3].

Focusing on the information storage capabilities of a memristor network, in this work we are investigating the enhancement of system's performance by increasing the variability tolerance of memristor-based memory using external additive noise signals. As source of inspiration, the non-linear system phenomenon known as Stochastic Resonance (SR) [4] indicates that a proper noisy disturbance can act in a beneficial manner for the performance of a non-linear system. Memristor constitutes a fine example of non-linear system, thus SR for the enhancement of its capabilities, such as its maximum to minimum resistance ratio, has been already studied [5]. Hence, going beyond the standalone device, here, a memristor network using the crossbar array configuration for dense and low-power memories is adopted. The Bit Error Rate (BER), as performance measure, is studied against the beneficial effects of external additive noise. In particular, temporal variability, spatial variability and their combination have been included in a small memristor-based crossbar array, where a physics-based ReRAM model is utilised for accurate and realistic simulation. The effect of external noise with varying intensity is taken into account and promising results for strongly reduced BER are presented, leading to variability-aware design of memristor-based memories.

II. Memristor-based Cell and Memristor Crossbar

The modelling of two-terminal thin-film devices, such as the ReRAM devices, is yet a non-trivial procedure; there are numerous models in the literature arriving from different disciplines and considering diverse approaches (physics-based, phenomenological, etc.) [6], [7]. In the context of this paper, Stanford-PKU ReRAM device model [8] has been utilised for performing the memristor devices simulations. This is owing to the fact that this physics-based model has been extensively employed in numerous simulations providing a concrete basis for comparison analysis; moreover, also due to its modelling characteristics, it has been reported that can accurately describe the behaviour of actual oxide-based ReRAM devices by modelling the conductive filament's (CF) growth within the insulating layer of the device. In more details, the model considers both the development of the gap distance and the width of the CF to feature the ReRAM's device resistive switching. Thus, when a positive voltage is applied on the device, the CF is growing and the total resistance is driven to the low resistance state (R_{ON}), namely the SET process. On the contrary, when a negative voltage is applied on the device, the CF is disrupted and, as a result, the device ends up to high resistance state (R_{OFF}) issuing the so called



(a) (b)

Fig. 1. The 1T1R ReRAM-based memory cell and its SET and RESET processes.

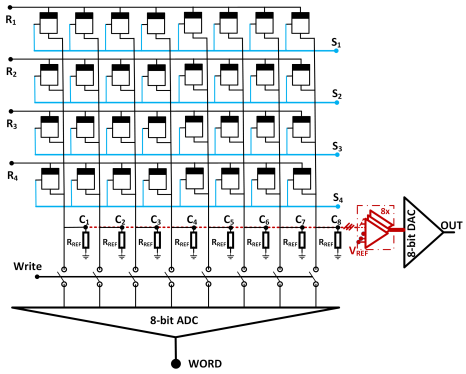


Fig. 2. ReRAM crossbar array with the read/write peripheral circuitry.

RESET process. In specific, for the aforementioned Stanford-PKU ReRAM device model, the RESET and SET processes can be performed by applying negative and positive pulses, respectively, with amplitude $V_{PULSE} = |2|$ V and pulse width $\tau = 80$ ns. Also, the rising and falling edge duration of each pulse were set to $\tau_{r/f} = 10$ ns, resulting to a total of 100 ns per pulse. A few details on the proposed model's operation can be found in Fig. (Fig. 1) where the SET and RESET processes of a 1T1R ReRAM cell are depicted.

In addition, parasitic elements are included for the encapsulation of the switching layer's and electrodes' parasitic resistances and the parasitic capacitance between the electrodes. Furthermore, one of the most significant features of this model is its capability to include device's current fluctuations by the introduction of stochastic processes during the growth of the CF, causing the cycle-to-cycle variation of the device and results to increased BER of the ReRAM-based memories.

Incorporating the abovementioned ReRAM device to a ReRAM network, the functionality and the circuitry of a memristor-based crossbar array for the storage of information is explored. For readability and presentation reasons, a 4×8 crossbar array is designed, where in each cell, logical '0' (logical '1') is mapped to device's high (low) resistive state. Along with the memristor, a selector transistor [9] is included in each cell to restrict the effect of the sneak path problem dominant in passive memristor networks [10] (Fig. 1(a)). Additionally, the reversed polarised memristor is advantageous during the read and write processes in the crossbar.

Since the resistance value cannot be read directly, the reading process comprises a short-amplitude positive pulse that

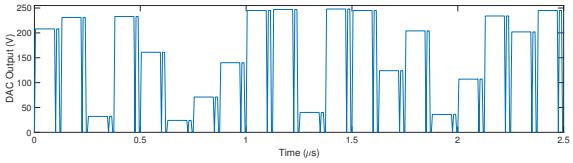


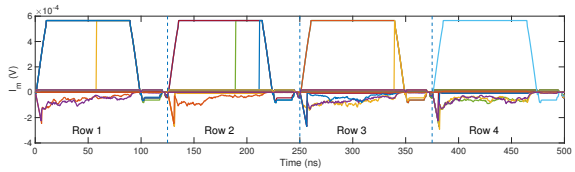
Fig. 3. Output of the DAC, depicting the writing (long pulses) and the reading (short pulses) of words in the crossbar array.

maps the resistive state to the corresponding voltage with the assistance of a reference resistor $R_{REF} = 100K\Omega$, based on the voltage divider as depicted in Fig. 2. In further details, the write and read processes in the memristor crossbar are performed in a row-based manner, so the 8-bit word can be written/read simultaneously. Thus, to write/read a 8-bit word, a $V_{SEL} = 5$V pulse is applied to the S_i terminal, where i is the selected row, while in the same time the proper signals are applied to the R_i and C_{1-8} terminals.

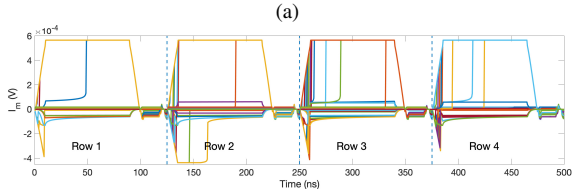
During the writing process, a positive $V_{RST} = 2$V pulse is applied to the selected row, able to RESET all the cells of the row. At the exact moment, the amplitude at the $WORD$ signal is sampled by the Analog-to-Digital Converter (ADC) found at the bottom of Fig. 2, and the corresponding 8-bit word is applied to the columns, one bit per column. The output of the ADC is $V_0 = 0$V for logical '0' bits and $V_1 = 4$V for logical '1' bits. Consequently, when the ADC generates a logical '0', the V_{RST} affecting the R_i is capable of RESET the device, illustrated in the first half of Fig 1(b). In case of logical '1', the $V1$ surpasses the V_{RST} and it is strong enough to SET the device, as presented in the second half of Fig. 1(b). Having the memristor reverse polarised, the 8-bit word is directly written to the cell of the row, while in the case that memristor was forward polarised, then additional inversion of the ADC's output would be required.

For the read process, a $V_{READ} = 1V$ pulse with shorter duration than the write pulses is delivered to the selected row R_i, while the $WRITE$ switches are open so the read pulses are driven to the R_{REF} resistors. The voltage on the R_{REF} resistors is sensed by one comparator per column, which have $V_{REF} = V_{READ}/2 = 0.5$V. Finally, the outputs of the comparators are connected to a Digital-to-Analog Converter (DAC), as shown in the right part of Fig. 2, and the read word is translated to a decimal number. The reversed polarisation of the memristor, here, protects against unwanted switching of the device as the reading pulse could RESET the device but when R_{ON}, the voltage is mostly dropped on the R_{REF} due to the voltage divider.

Throughout the simulations, after a write process, the selected row is always read to evaluate the successful writing of the word. The long duration pulses in Fig. 3, which depicts the DAC's output, are caused during the write process by the ADC's output and correspond to the word that is written in the crossbar; however, the following short pulses come from the read-out of the previously written word to verify its proper writing. All the simulations have been held using the SPECTRE simulator in the Cadence Virtuoso platform. It should be also mentioned in the context of the presented simulations, all



(a)



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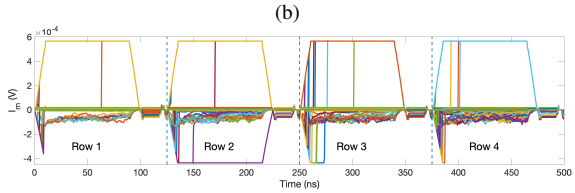

(c)

Fig. 4. SET and RESET variations under the effect of (a) temporal, (b) spatial and (c) temporal and spatial variability. The variations are illustrated by the varying behaviour of current through each memristor device of the array.

the peripheral circuitry elements are considered to be ideal. As a result, energy and area efficient design of the peripheral circuits needs to be further studied.

III. Variability

Although the high density of crossbar architecture provides unique capabilities for memristor-based applications, the manufactured devices show increased levels of differentiation between the devices of the crossbar array (device-to-device), as long as there are also variations on the switching kinetics of a unique device after identical writing signals are applied (cycle-to-cycle). Both of them are affecting proper function of the writing process of the memristor-based memories and as a result, they are increasing the Bit Error Rate (BER) of the memristive system. BER is calculated as the portion of faulty written bits out of the total number of bit writings, i.e. if 1 bit is erroneous after the writing of one row (word) then BER$= 1/8 = 12.5\%$.

Temporal Variability. The Stanford-PKU memristor model incorporates the temporal variability of a device using two random processes, one for the gap state variable and the other for the CF width. The effect of those two processes can be adjusted by the variables $\{\delta_g, \delta_r\}$, respectively [8]. Aiming to introduce the temporal variability and set-up a level of BER as a benchmark, the aforementioned parameters were swept and for $\{1, 2.5\}$ the BER of 10.54% measured for 3,000 consecutive writings. For the accurate evaluation of temporal variability's effect, long-time simulations with large number of consecutive pulses are required. Limited samples of those writings are detailed in Fig. 4(a), where the switching of all the memristors, row-after-row, is depicted through the memristors' currents.

Spatial Variability. Furthermore, to incorporate also the spatial variability of the crossbar array, Monte Carlo simulations are performed where a statistical process for devices' mismatch is applied. In specific, during each simulation, a different set of activation energies for SET (E_i) and RESET (E_a) of each device was selected from a Gaussian distribution with mean value the nominal value of each parameter and standard deviation 40% of this value. In such a way, the average BER including spatial variability in the crossbar reached the 7.51% for 20 simulations of 100 consecutive writings each. Here, the number of repetitions of the same simulation with different device's characteristics is crucial and needs to be large enough for the proper evaluation of spatial variability's effect in the crossbar. In similar way to the temporal variability case, here, Fig. 4(b) shows the varying switching of all memristors in the grid for 10 example simulations with device mismatch. The effects of combined temporal and spatial variability at the switching of the devices are illustrated in Fig. 4(c), while the outcome of variability at the proper writing of words in the rows of the crossbar is illustrated in the example of Fig. 5.

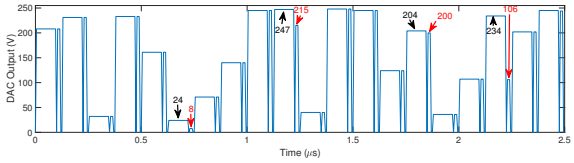

Fig. 5. Example of DAC's output with erroneous written words. Desired words are pointed by the black arrows and erroneous outcomes by the red arrows.

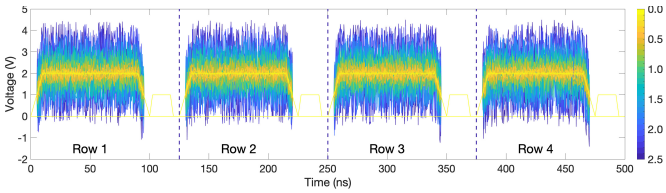

Fig. 6. Examples of voltage applied on each row for different levels of noise intensity.

IV. Noise Induced BER Reduction

Aiming to restrict the negative effect of variability in novel ReRAMs, the stochastic resonance phenomenon is investigated for the memristor crossbar array described above. In more details, additive zero-mean Gaussian noise with varying noise intensity (V_{NOISE}) is applied along with the write pulse of each row. Fig. 6 illustrates examples of the noisy voltages that are applied on each row during writings. The color of each line is related with its V_{NOISE}, following the colorbar.

Firstly, the effect of additive noise on a memristor crossbar with only temporal variability is studied. Fig. 7(a) shows the measured BER for a sweep of the noise's amplitude in the range $V_{NOISE} = \{0, 0.1, ..., 2.5\}$V, where, for each case, 3,000 consecutive random 8-bit words were written into the crossbar, one word per row and row-after-row. The resulting trend shows clearly the positive effect of additive noise as it is able to diminish the BER down to 0.0708% for $V_{NOISE} = 1.8$V. As expected, additional increase of noise results to BER increase, since noise is switching the device uncontrollably.

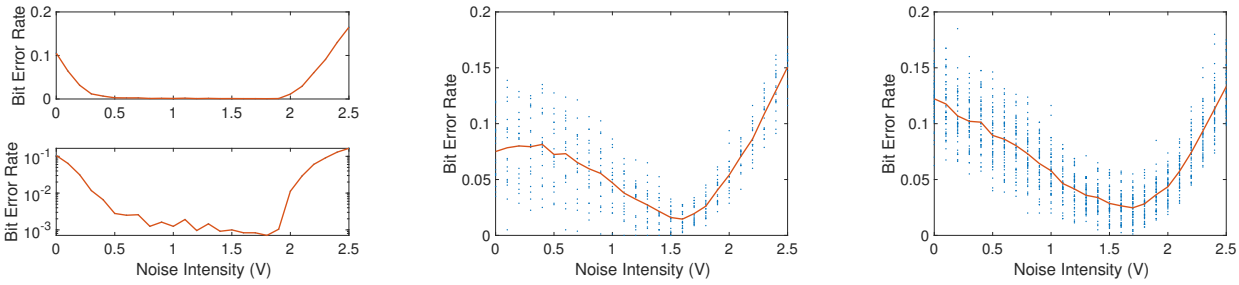

Fig. 7. The trend of BER against the intensity of externally applied noise for (a) temporal, (b) spatial and (c) combination of temporal and spatial variability. In (a), the BER is presented in both linear and logarithmic scale for further clarification of the minimum BER point.

Going further, additive noise sweeps are performed on crossbar arrays with only spatial variability taken under consideration. Here, for every V_{NOISE}, a set of 20 simulations with varying SET and RESET thresholds for each device is performed, where in each simulation 100 words were written in the same manner as in the temporal variability case. Fig. 7(b) presents the measured BER for each simulation, along with the BER mean value trend, showing its average reduction down to 1.46% for $V_{NOISE} = 1.6$V.

Finally, the combination of temporal and spatial variability was explored, where the average BER without the incorporation of additive noise reaches 12.22%. Fig. 7(c) shows the measured BER of 50 simulations at each point of noise intensity for 100 word writings under the aforementioned cycle-to-cycle variability and also varying SET and RESET thresholds of each device. The mean value trend of BER is illustrating the reduction of the average BER down to 2.47% at $V_{NOISE} = 1.7$V. The increased number of simulations, here, aims to increase the credibility of the presented results for the most realistic case of the study, where both temporal and spatial variability are incorporated, considering larger number of different devices that can be found in bigger crossbar arrays.

V. Conclusions

Memristor-based crossbar arrays constitutes the strongest candidates for novel ultra-dense memories and in-memory computing. Compared to the nano-crossbar arrays which have emerged as a strong candidate technology to replace CMOS in near future [11], integrate well developed conventional circuit design techniques [12] and result to the design and construction of emerging nanocomputers, memristor crossbars are one the most promising alternatives due to their unique characteristics. However, the high levels of fabricated memristor's variability postpones the scaling of actual memristor-based memories. In a crossbar, the differentiation between the switching characteristics of each device is evident, along with the inability to replicate the switching of an individual device cycle-after-cycle. In this work, both of the aforementioned problems are investigated in a small 4-row crossbar with 8-bit words per row, considering the readability of this work. Furthermore, the utilisation of the noise-related phenomenon of Stochastic Resonance on the crossbar array has been studied. The introduction of the proper additive noise signal during the writing of the 8-bit words shown that, under specific conditions, the writing process of the devices can be assisted by a noisy disturbance and the total Bit Error Rate of the array will be significantly reduced.

Acknowledgment

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