High CMRR Current Mode Operational Amplifier with a Novel Class AB Input Stage

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ABSTRACT
In this paper, improved CMRR, high gain CMOS current-mode operational amplifier (COA) is presented. A new class AB input stage is used in order to obtain very low input resistance. The proposed COA is operated under ±1.5 V voltage supplies and designed with 0.35-μm CMOS process. Results of simulation indicate a 107 dB DC gain, 123 Ω input resistance, common mode rejection ratio exceeding 110dB and a gain-bandwidth product at about 100 MHz.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *VLSI (very large scale integration).*

General Terms: Design

Keywords
Current-mode circuits, current-mode operational amplifier

1. INTRODUCTION
Current-mode signal processing has attracted more attention in recent years because current-mode circuits provide several advantages over its voltage-mode counterparts, such as high frequency capability, wide dynamic range and simple circuitry with lower voltage supplies [4, 7]. Several current-mode building blocks have been suggested in the literature and some of them are commercially produced, e.g. current conveyors and current feedback operational amplifiers. Current-mode operational amplifier (COA) is another useful current-mode integrated building block. It is the attractive feature of using COA that by applying adjoint network principle, almost all transfer functions implemented with conventional voltage operational amplifiers (VOA) can be alternatively implemented with COA's [3].

COA ideally exhibits zero input resistance and infinite output resistance and current gain. The circuit symbol and the equivalent circuit are reported in Fig.1. While designing a COA, input resistance enhancement is usually difficult. To decrease the input resistance, some complicated negative feedback configurations have been presented [6, 5]. However, these improvement methods generally worsen the frequency response of the COA and are not easily applicable to class AB input stages. Positive feedback is another solution to get lower input resistance and it has simpler circuitry [8, 2]. Although [8] provides low input resistance in class AB operation, it suffers from the stability of quiescent current. This paper presents a novel positive feedback approach used in class AB input stage.

Folded-cascode op-amp gives efficient performance as a current output stage [1]. In this study, due primarily to the larger bandwidth and slew rate, the current-mirror op-amp is preferred instead of a folded-cascode one. Furthermore, wide-swing current source is used in the output stage for CMRR improvement. Thus, we could achieve good CMRR performance with only changing the type of a current source.

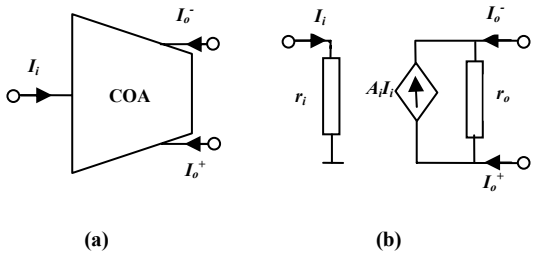

Figure 1. (a) Circuit symbol (b) Equivalent circuit

2. PROPOSED COA
CMOS realization of the proposed COA is shown in Fig. 2. The amplifier is configured from a single input transimpedace stage followed by a differential output transconductance stage. Compensation capacitance (Cc) is inserted at the high impedance node series with M17 which operates like a resistance and improves frequency response of the COA. W/L of transistors and DC values of the circuit are reported in Table 1 and Table 2 respectively. In the following subsections we will study on input and output stages.

2.1 Input Stage of the Proposed COA
Each of the transistors M1 and M4 operates as a current source and determine the quiescent current. Shown in dashed lines M10, M6 and M8, M13 compose positive feedback loops to reduce input resistance and enable zero DC voltage at the input.

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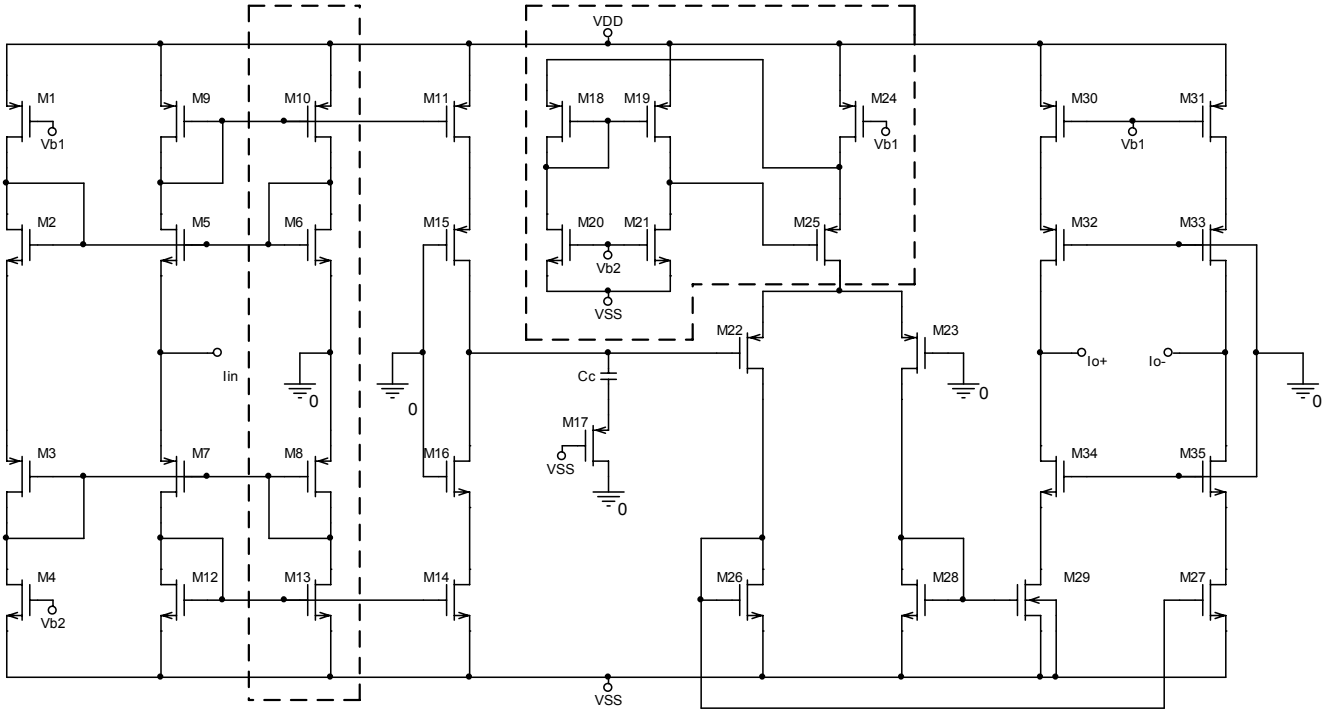

Figure 2. Schematic of the proposed COA

Because, only four more transistors are used for input resistance improvements, frequency response of the amplifier is not noteworthy affected by these additional transistors. Equations (1) shows input resistances without positive feedback loops and generally its value is not low enough.

$$r_{in} \cong \frac{1}{g_{m5} + g_{m7}} \tag{1}$$

Input resistance equations of the proposed COA are shown in (2), (3) and (4). The second terms of (3) and (4) play an important role in reducing input resistance. If we select their values close to zero, r_{in} also goes near zero. Moreover, their values must bigger than zero to overcome the stability problem. If we choose g_{m5}=g_{m6}, g_{m9}=g_{m10} and g_{m7}=g_{m8}, g_{m12}=g_{m13}, then we will both overcome stability problem and obtain very low input resistances. Consequently we come such a decision that $(W/L)_{M5}$=$(W/L)_{M6}$, $(W/L)_{M9}$=$(W/L)_{M10}$, $(W/L)_{M7}$=$(W/L)_{M8}$, $(W/L)_{M12}$=$(W/L)_{M13}$. On the other hand, it is undesirable that input resistance value is very sensitive to some parameters. As, accurately determining the effects of these parameters on input impedance needs very detailed study, just MOS transistor matching parameters are considered in this paper. To analyze the MOS transistor mismatches, firstly we need to calculate variances of relative current gain factor (K) mismatch- σ(ΔK/K)- and threshold voltage (VT) mismatch- σ(ΔVT)- for transistors M5-13. As it will be reported in the 'Simulation Results' part, input resistance stays positive while considering the matching parameters in worst case.

$$r_{in} = r_{in1} // r_{in2} \tag{2}$$

$$r_{in1} \cong \frac{1}{g_{m5} g_{m9}} \left[\left(g_{ds5} + g_{m9} + g_{ds9} \right) - \frac{g_{m5} g_{m10}}{g_{ds10} + g_{m6} + g_{ds6}} \right] \tag{3}$$

$$r_{in2} \cong \frac{1}{g_{m7} g_{m12}} \left[\left(g_{ds7} + g_{m12} + g_{ds12} \right) - \frac{g_{m7} g_{m13}}{g_{ds13} + g_{m8} + g_{ds8}} \right] \tag{4}$$

2.2 Output Stage of the Proposed COA

Current-mirror op-amp is selected as an output stage. For this stage the K factor is explained as a current gain from the input transistors (M26 and M28) to the output sides of the current mirrors connected to the output node.

$$K = (W/L)_{M29} / (W/L)_{M28} = (W/L)_{M27} / (W/L)_{M26} \tag{5}$$

Compared to the folded-cascode structure, being able to select different K values offers some advantages. For instance, for the constant output current range, increasing K implies lower power dissipation and better bandwidth. K=3 is selected in this design. From equation (6), it can be inferred that CMRR of the amplifier is extremely dependent on output resistance of the current source in dashed lines. This proposed current source provides very high output resistance compared to the simple and cascode current sources. Output resistance equations of simple, cascode and proposed current-mirror are given by (7), (8) and (9) respectively.

$$CMRR = \frac{A_d}{A_c} \cong g_{m22,23} r_{outCS} \tag{6}$$

$$r_{outCS1} = \frac{1}{g_{ds24}} \tag{7}$$

$$r_{outCS2} \cong \frac{g_{m25}}{g_{ds24} g_{ds25}} \tag{8}$$

$$r_{outCS3} \cong \frac{g_{m25} g_{m19}}{g_{ds24} g_{ds25} (g_{ds19} + g_{ds21})} \quad (9)$$

Output resistance of the COA is shown in equation (10).

$$r_{out} \cong \left[\frac{g_{ds34,35} g_{ds27,29}}{g_{m34,35}} + \frac{g_{ds32,33} g_{ds30,31}}{g_{m32,33}} \right]^{-1} \quad (10)$$

DC current gain and gain-bandwidth product of the proposed COA are given by (11) and (12) respectively.

$$A_i(0) \cong K \frac{g_{m22,23}}{2} \left[\frac{g_{ds15} g_{ds11}}{g_{m15}} + \frac{g_{ds16} g_{ds14}}{g_{m16}} \right]^{-1} \quad (11)$$

$$f_{GBW} \cong \frac{1}{2\pi} K \frac{g_{m22,23}}{2Cc} \quad (12)$$

3. SIMULATION RESULTS

SPICE is used for simulation with the process parameters of a 0.35 μm CMOS technology. BSIM3 parameter sets are used for modelling transistors of which threshold voltages are nearly 0.5 V for NMOS and -0.7 V for PMOS. The transistor widths range from 5 to 140 μm.

Table 1. Transistor dimensions

Transistor	W(μm)/L(μm)	Transistor	W(μm)/L(μm)
M1	6/1	M20	2.8/2.8
M4	5/1	M21	14/2.8
M2,5,6	15/0.7	M22,23	60/0.7
M3,7,8	10/0.7	M24	60/1.4
M9, 10,11	15/1	M25	140/1.4
M12,13,14	7/1	M26,28	15/0.7
M15	50/1	M27,29	45/0.7
M16	9/1	M30,31	85/1.4
M17	15/07	M32,33	80/1.4
M18	50/2.8	M34,35	20/1
M19	10/2.8		

Table 2. DC values of the COA

Parameter	Value
$V_{DD} - V_{SS}$	+1.5 V, -1.5V
V_{b1}, V_{b2}	0.5V, -0.8V
I_{D1}, I_{D4}, I_{D5}, I_{D7}	10uA
I_{D22}, I_{D23}	40uA
I_{D29}, I_{D30}	120uA

Fig. 3 compares input impedance characteristics of conventional and proposed class AB input stages. Up to nearly 10 MHz, proposed circuit has much lower input resistance (123Ω). For transistors M5-13, 3σ(ΔVT) values are calculated between 6mV - 9mV and 3σ(ΔK/K) values are calculated between 0.5% - 1.2%. As a result, input resistance becomes +9 Ω for the worst case (still positive).

The CMRR behavior of the circuits is illustrated in Fig. 4. Curve a, b and c show a DC value of 113, 68 and 42 dB, respectively. The CMRR magnitude exhibited by case (a) results better than that of case (b) and (c) up to ≈20 MHz. Open loop frequency characteristic is seen from Fig. 5. The transient response to a step input current of ±100μA is shown in Fig. 6.

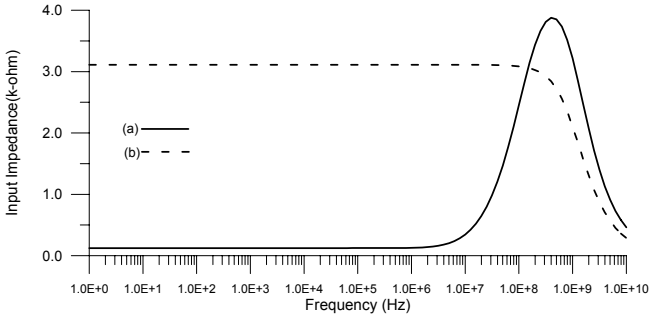

Figure 3. Magnitude of the input impedance of:

(a) Proposed class AB input stage

(b) Conventional class AB input stage

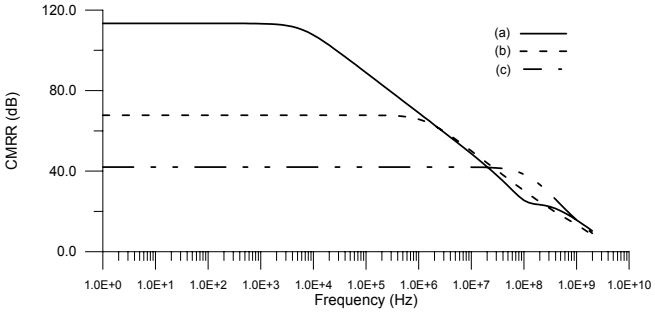

Figure 4. Magnitude of the CMRR of:

(a) Proposed COA-using wide swing current source

(b) The COA-using cascode current source

(c) The COA-using simple current source

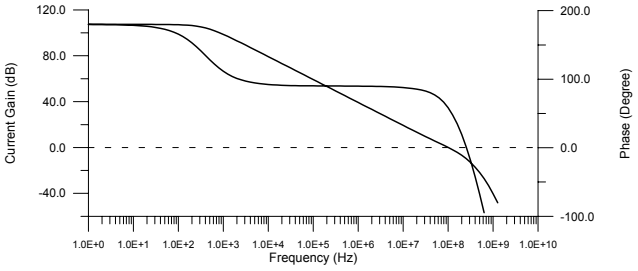

Figure 5. Open-loop frequency response of the COA

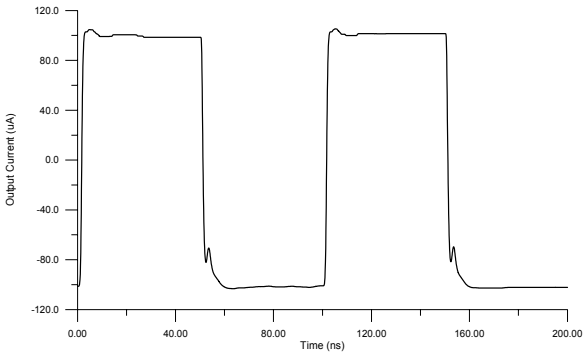

Figure 6. Response of the COA in unity-gain feedback to a ±100 µA input step (f=10MHz)

Table 3. Performance parameters of the COA

Parameter	**Value**
Power Dissipation	1.15 mW
Open-Loop Gain	107 dB
GBW	102 MHz
Phase Margin(Cc=0.8p Rc=2kΩ)	60˚
Output Voltage Range	±0.7 V
Slew Rate	163uA/ns
Input Resistance	123 Ω
Output Resistance	14 MΩ
CMRR	113 dB
Input Voltage Offset	≈ 1.6 mV

Table 3 summarizes the performance of the COA. The COA provides 107 dB dc gain, 102 MHz GBW, 112 dB CMRR and 60˚ phase margin guaranteeing single pole behavior throughout the unity gain bandwidth. Input and output resistance values are also fairly good.

4. CONCLUSION

In this work, very accurate COA is proposed and simulation results are presented. As expected from a COA, the circuit exhibits a high open loop gain, a high output resistance and a low input resistance. A novel class AB input stage that enables very low input resistance is used and also very high CMRR is achieved by choosing proper current source. Due to the simple circuitry of the proposed COA, higher than 100 MHz GBW is obtained. It also offers nice slew rate and ±0.7V output voltage swing.

These performance parameters demonstrate the reason of using the proposed COA instead of a conventional amplifier (VOA) in application circuits, such as active filters, oscillators and current-voltage amplifiers.

5. REFERENCES

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