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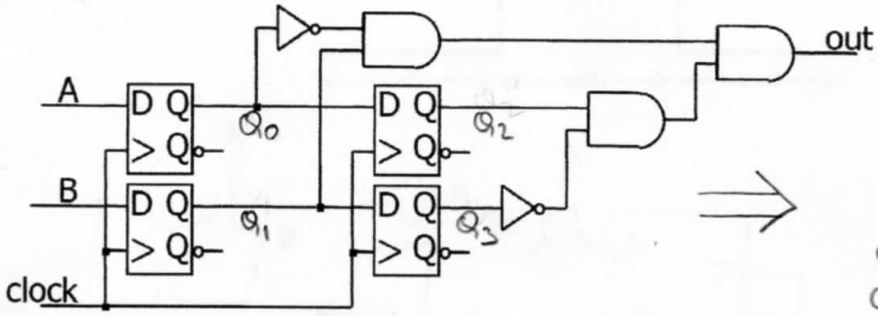
Student ID:

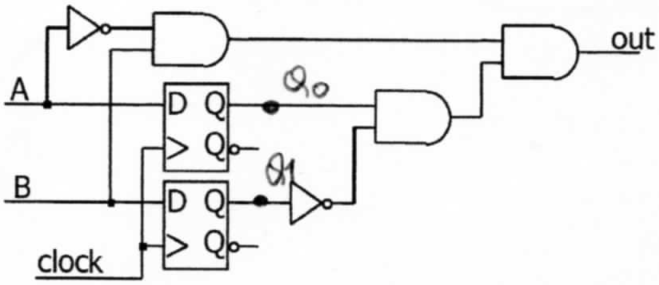
BLG231E Digital Circuits
Homework 3

Deadline: 30/12/2016 (before 9:30)

1. SEQUENTIAL CIRUITS: CITCUITS TO STATES

Consider sequential circuits shown below.





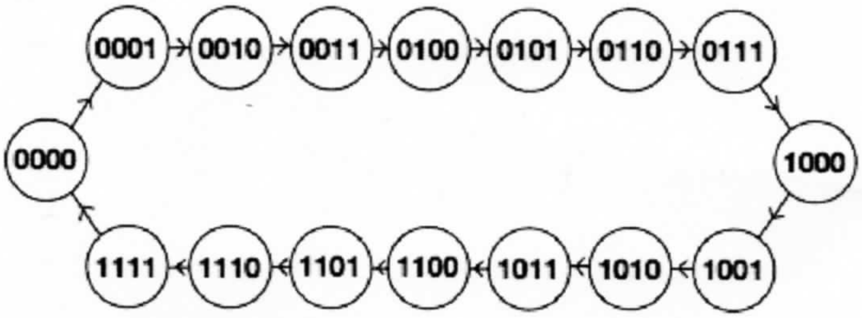
1) a) State Table of 1st Circuit

A	B	Q_0^c	Q_1^c	Q_2^c	Q_3^c	Q_0	Q_1	Q_2	Q_3
0	0	0	0	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	1
0	0	1	0	X	X	0	0	1	0
0	0	1	1	X	X	0	0	1	1
0	1	0	0	X	X	0	1	0	0
0	1	0	1	X	X	0	1	0	1
0	1	1	0	X	X	0	1	1	0
0	1	1	1	X	X	0	1	1	1
1	0	0	0	X	X	1	0	0	0
1	0	0	1	X	X	1	0	0	1
1	0	1	0	X	X	1	0	1	0
1	0	1	1	X	X	1	0	1	1
1	1	0	0	X	X	1	1	0	0
1	1	0	1	X	X	1	1	0	1
1	1	1	0	X	X	1	1	1	0
1	1	1	1	X	X	1	1	1	1

a) Obtain **state diagrams** and **state tables** of these two circuits.
b) Determine whether these circuits are **Mealy** or **Moore** machines.
c) Find the input conditions these circuits aim to recognize.
d) Explain the differences in terms of working principles of these two circuits.

2. SEQUENTIAL CIRUITS: STATES TO CIRCUITS

Consider a state diagram shown below. Implement this state diagram using T (toggle) flip-flops and AND gates. What is the purpose of the circuit?



1- a) continues

State Table Of 2nd Circuit

A	B	Q_0^c	Q_1^c	Q_0	Q_1
0	0	X	X	0	0
0	1	X	X	0	1
1	0	X	X	1	0
1	1	X	X	1	1

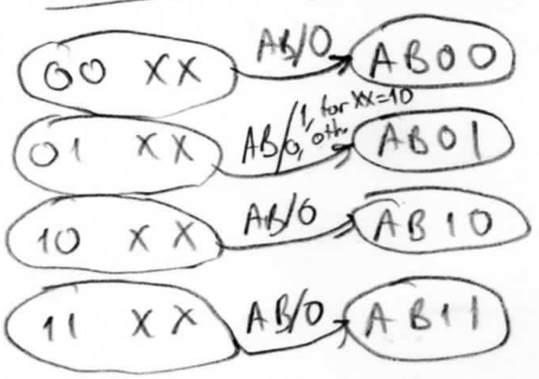
Output Truth Table of 1st Circuit

Q_0^c	Q_1^c	Q_2^c	Q_3^c	out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

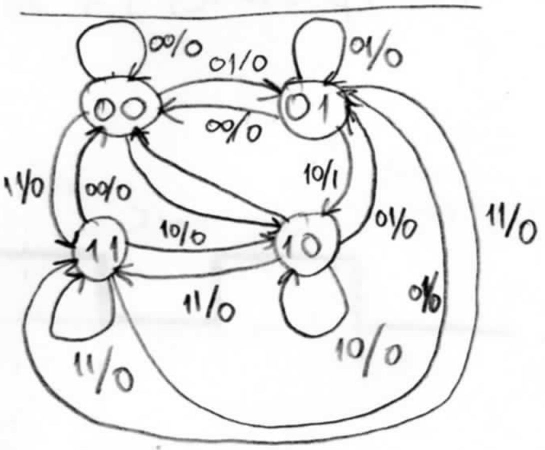
Output T.T. of 2nd Circuit

A	B	Q_0	Q_1	out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

State Diagram of the 1st Circuit



S.D. of the 2nd Circuit



b) 1st Circuit ⇒ Moore machine, output depends only on current states

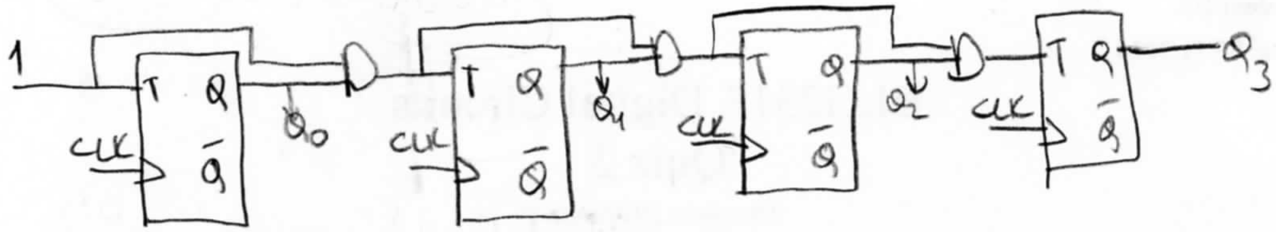
2nd Circuit ⇒ Mealy machine, output depends on both current input and current states.

c) 1st Circuit ⇒ The circuit aims to recognize when previous input is 01 and current Q_2Q_3 is 10

2nd Circuit ⇒ Aiming to recognize when the current input is 01 and current Q_0Q_1 is 10.

d) In 1st circuit, the inputs only determines the next state, output is only determined by current states. However, 2nd circuit uses inputs for determination of both outputs and next states.

2-) It is an up counter circuit. Up counter with T-FFs and AND gates:



Q_3^C	Q_2^C	Q_1^C	Q_0^C	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

3–

Grouped by output

		X=0	X=1	Z
①	a	①	②	1
	b	②	②	1
	c	②	②	1
	e	①	②	1
	j	①	②	1
②	d	①	①	0
	f	①	①	0
	h	①	①	0
	i	①	①	0

⇒ Re-Grouped By NextStates

		X=0	X=1	Z
①	a	②	③	1
	e	①	③	1
	j	②	③	1
②	b	③	③	1
	c	③	③	1
③	d	①	①	0
	f	①	②	0
	h	①	②	0
	i	①	②	0

⇒ Re-Grouped By N.S.

		X=0	X=1	Z
①	a	③	⑤	1
	j	③	⑤	1
②	e	②	⑤	1
③	b	⑤	⑤	1
	c	⑤	⑤	1
④	d	①	⑤	0
⑤	f	①	③	0
	h	①	③	0
	i	①	③	0

(This table does not need to be re-grouped)

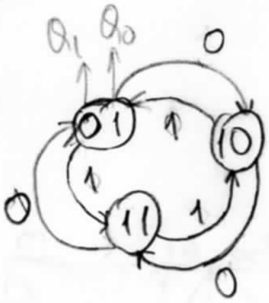
So minimum 5 states is needed.

① → a
② → e
③ → b
④ → d
⑤ → f

	X=0	X=1	Z
a	b	f	1
b	f	f	1
d	a	e	0
e	e	f	1
f	a	b	0

(Reduced state table)

4 – a)



Q_1^C	Q_0^C	I	Q_1	Q_0
0	0	0	X	X
0	0	1	X	X
0	1	0	1	0
0	1	1	1	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Q_0

I \ $Q_1^C Q_0^C$	00	01	11	10
0	X	0	1	1
1	X	1	0	1

$Q_0 = \overline{Q_0^c} + \bar{I}.Q_1^c + I\overline{Q_1^c}$

Q_1

I \ $Q_1^C Q_0^C$	00	01	11	10
0	X	1	0	1
1	X	1	1	0

$Q_1 = \overline{Q_1^c} + I.Q_0^c + \bar{I}.\overline{Q_0^c}$