Power-Delay-Area Performance Modeling and Analysis for Nano-Crossbar Arrays

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***Abstract*— In this study, we introduce an accurate capacitor-resistor model for nano-crossbar arrays that is to be used for power/delay/area performance analysis and optimization. Although the proposed model is technology independent, we explicitly show its applicability for three different nanoarray technologies where each crosspoint behaves as a diode, a FET, and a four-terminal switch. In order to find related capacitor and resistor values, we investigate upper/lower value limits for technology dependent parameters including doping concentration, nanowire dimension, pitch size, and layer thickness. We also use different fan-out capacitors to test the integration capability of these technologies. Comparison between the proposed model and a conventional simple one, which generally uses one/two capacitors for each crosspoint, demonstrates the necessity of using our model in order to accurately calculate power and delay values. The only exception where both models give approximately same results is the presence of considerably low valued resistive connections between switches. However, we show that this is a rare case for nano-crossbar technologies.**

Keywords—Nano-crossbar array; circuit modeling; performance analysis; emerging technologies; post-CMOS

I. INTRODUCTION

Nano-crossbar arrays have emerged as a strong candidate technology to replace CMOS in near future [1-3]. They are regular and dense structures, and fabricated by exploiting self-assembly as opposed to purely using lithography based conventional and relatively costly CMOS fabrication techniques [4-6]. Currently, nano-crossbar arrays are fabricated such that each crosspoint can be used as a conventional electronic component such as a diode [7], a FET [8], or a switch [9]. This is a unique opportunity that allows us to integrate well developed conventional circuit design techniques into nano-crossbar arrays. However, as expected the integration comes with some challenges and the accuracy problems in performance modelling and analysis is one of the significant ones. Conventional resistor-capacitor models do not meet the needs of nanoarrays [10-13]. They generally neglect wiring resistors/capacitors including crosstalk capacitors with an assumption that their values are much smaller than those of device resistors/capacitors. However, this is not applicable for nanoarrays where both devices and wirings between them are implemented using the same physical substrate such as nanowires or nanotubes. Another important factor is that as opposed to conventional two-terminal switch based devices such as diodes and transistors that conduct current in one direction, nano-crosspoint switches with four neighbor crosspoints can conduct current in four directions that certainly needs a different model.

In this study, we propose an accurate capacitor-resistor model for nano-crossbar arrays that is used for power/delay/area performance analysis and optimization. Although the proposed model is technology independent, it can be applicable for variety of emerging technologies including nanowire crossbar arrays [5], molecular crossbar arrays [14], memristive arrays [15], and multi layered nanoarray structures such as CMOL [16-17]. We explicitly show the model's applicability for three different nanowire based technologies where each crosspoint behaves as a diode, a FET, and a four-terminal switch [7-9]. Fig. 1 illustrates these three types.

Exploiting the developed models for diode, FET, and four-terminal switch based arrays, we perform power-delay-area performance analysis and optimization. To calculate related capacitor and resistor values, we use upper/lower value limits for the parameters of doping concentration, nanowire dimension, pitch size, and layer thickness. We also use different fan-out capacitors to test the integration capability of these nanowire based technologies. Indeed, if all parts of a computing system could be satisfactorily and preferably realized with nano-crossbar arrays as opposed to CMOS then there would be no need for integration, so even terahertz frequency levels would be achievable. However, the current state-of-the art has not reached this point [1, 18], so the integration with CMOS is a must. We simulate this by using relatively large fan-out capacitors.

Previous studies on performance modeling and analysis of nanoarrays lack of accuracy and comprehensiveness. Capacitor-resistor models and their parameter values are determined with weak assumptions without in depth analysis of nano-array technologies [10]. Additionally, some studies exploit current or predictive technology models for nanoscale CMOS which certainly has major differences from nanoarray based technologies, both in design and manufacturing levels [12, 19-21]. In this study, we aim to overcome these shortcomings by introducing accurate modeling and performance analysis techniques for nano-crossbar arrays.

The paper is organized as follows. In Section 2, we propose our technology independent capacitor-resistor model for nano-crossbar arrays. Using the model, we develop performance analysis models and techniques for diode, FET, and four-terminal switch based nanoarrays. In Section 3, we perform calculations for needed technology parameters and obtain power-delay-area analysis results and inferences. In Section 4 we evaluate our capacitor-resistor model given in Section 2. In Section 5, we perform performance analysis of a 1-bit full adder and a memory array using nanowire crossbar arrays. In Section 6, we present conclusions.

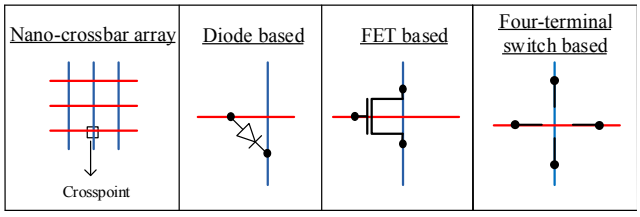


Fig. 1. A switching nano-crossbar array with diode, FET, and four-terminal switch based crosspoints.

II. CAPACITOR-RESISTOR MODELING OF NANOARRAYS

Nano-crossbar arrays are regular structures consisting of identical crosspoint cells. Fig. 2 illustrates a cell with the proposed capacitor-resistor placements. It consists of two crossed lines/wires with intersecting parts shown in green and nonintersecting parts shown in grey. The intersecting part is expected to behave as an electronic component such as a diode, a FET, or a switch. We model this part with wire resistors and four identical crosspoint capacitors C_{CP}'s. The reason of using four capacitors instead of one is the necessity of considering resistances between N_1-N_2 and N_3-N_4 nodes. Using a single crosspoint capacitor is only applicable if these resistances are negligibly small. For the nonintersecting parts, we use a wire resistor R_w and a wire capacitor C_w that is composed of parasitic wire, parallel wire, wire-layer, and wire-bulk capacitors. Other parameters defined are wire diameter D, layer thickness t_l (between wires), and pitch size p_w (distance between parallel wires).

We explicitly show our model's applicability for three different technologies of nanowire crossbar arrays where each crosspoint behaves as a diode, a FET, and a four-terminal switch as shown in the upper part of Fig. 2. Here, along with wire resistors we use switches having series ON and OFF parasitic resistances. For the diode-based crosspoint, it is assumed that the upper and the lower wires are *p*-type and *n*-type nanowires, respectively. The crosspoint is modeled with a switch, representation of a *pn*-diode four capacitors, and four wire resistors. For the FET based crosspoint, the layer between two wires acts as an insulator, so no current flows between the wires. The upper wire is modeled with a resistor and the lower wire is modeled as a switch controlled by the upper wire's voltage. Since the upper wire does not conduct current, N_1 and N_2 nodes are shorted that results in two crosspoint capacitors, each having a value of $2C_{CP}$. For the four-terminal switch based crosspoint, the upper and the lower wires are identically modeled using total of four capacitors and four switches. Here, current can flow in multiple directions. Comparison of these three models with neglected wire resistors is visualized in Fig. 3 (N_1-N_2: upper, N_3-N_4: lower).

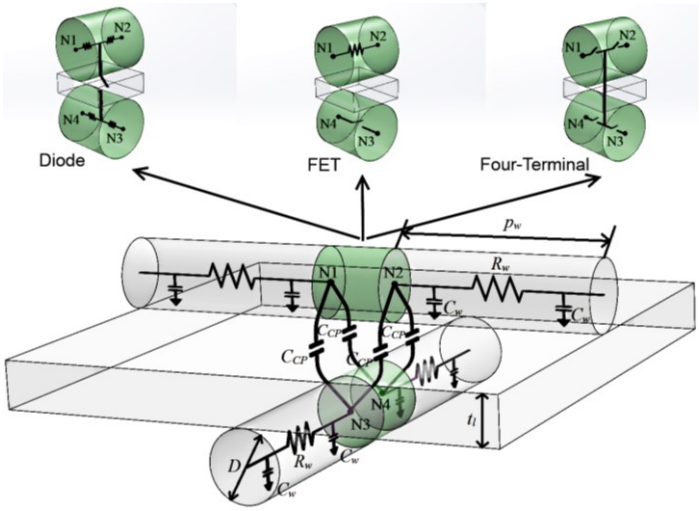


Fig. 2. A nano-crossbar cell and its different forms for diode, FET, and 4-terminal switch based nanowire crosspoints.

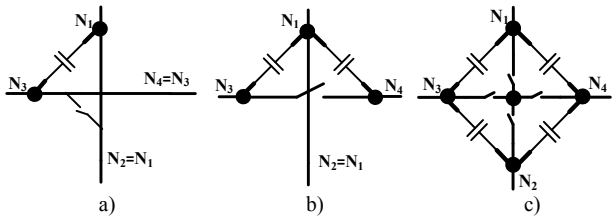


Fig. 3. Capacitor and switch placements for crosspoints based on a) diode, b) FET, and c) four-terminal switch (N_1-N_2: upper, N_3-N_4: lower).

A. Simplified power-delay model

We simplify our capacitor-resistor models with an aim of effectively using them for power and delay analysis. We transform in-between node capacitors C_{CP}'s, shown in Fig. 3, into grounded equivalent node capacitors C_{CP_eqv}'s that is to be compatible with the Elmore delay model [22]. Miller theorem is used for this purpose [23]. Equivalent grounded capacitors for C_{CP}'s are obtained with the formulas given in Fig. 4. Formulas are derived by exploiting the conservation of the capacitor charge $\boldsymbol{Q_C}$; recall that $\boldsymbol{I_C} = \boldsymbol{C} \times \frac{d\boldsymbol{V_C}}{d\boldsymbol{t}}$ and $\Delta\boldsymbol{Q_C} \cong \boldsymbol{C} \times \Delta\boldsymbol{V_C}$.

Our crosspoint model and its equivalent with grounded capacitors are shown in Fig. 5a) and Fig. 5b), respectively. There are two criteria for comparing these two models: 1) effectiveness of using them in power-delay analysis, and 2) accuracy and easiness of calculating related capacitor values. For the first criteria, the model in Fig. 5b) overwhelms the other; grounded capacitors are highly desired both in circuit simulations and hand calculations. However, things are reversed for the second criteria. Since we define C_{CP}'s with physical reasoning, we can calculate their values using technology parameters such as distances, concentrations, and physics constants. On the other hand, accurately calculating the values of C_{CP_eqv}'s necessitates to know node voltage values and this might not be practical regarding that node voltages are dynamically changing between a supply voltage and a ground, namely V_{DD} and GND = 0V.

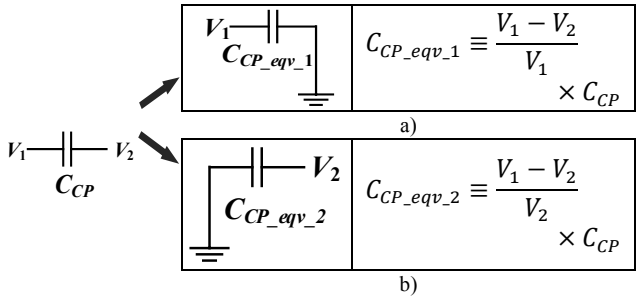


Fig. 4. C_{CP} and its equivalent capacitors a) $C_{CP\_eqv\_1}$ on V_1 and b) $C_{CP\_eqv\_2}$ on V_2.

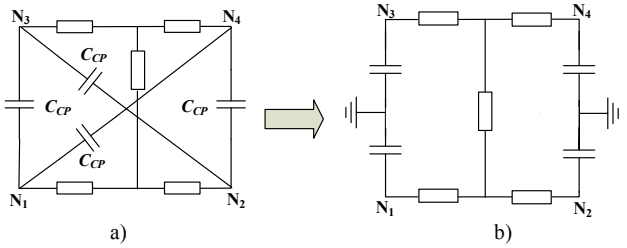


Fig. 5. Our crosspoint models using a) real crosspoint capacitors and b) their equivalent grounded capacitors.

In order to find equivalent capacitor values, we fundamentally use the formulas in Fig. 4. Since the formulas require node voltage values which are directly dependent on application circuits, we use a predetermined test circuit shown in Fig. 6. The test circuit comprises a single crosspoint and a load resistor. Equivalent crosspoint models using the test circuit are shown in Fig. 7. For the FET based crosspoint, input and output voltage changes can be negatively correlated. In other words, it is possible to simultaneously see GND-to-V_{DD} transition at the input and V_{DD}-to-GND transition at the output. Therefore each of the two equivalent grounded capacitors has a maximum value of $2\times2C_{CP}$=$4C_{CP}$. On the other hand, their minimum values are $2C_{CP}$ that is obtained when there is no transition at the output. As a result, two grounded capacitors can take values between $2C_{CP}$ and $4C_{CP}$. We choose an average value of $3C_{CP}$. This is illustrated in Fig. 7b). For the diode and four-terminal switch based crosspoints, we derive k_i values for capacitor values, in Fig 7d). Here, R_{W_CP}, R_{OFF}/R_{ON}, R_w, and R_L represent crosspoint wire resistor, crosspoint switch resistor, outside (crosspoint) wire resistor, and load resistor, respectively.

By using the developed models, we perform calculations for needed technology parameters and obtain power-delay-area analysis results and inferences in the following section**.**

III. Performance Analysis: Power, Delay, Area

In this section, we perform performance analysis for diode, FET, and 4-terminal switch based nanowire crosspoints by using the test circuit in Fig. 6 and the proposed crosspoint models in Fig. 7. For delay analysis, we use the Elmore delay formula regarding that all of the capacitors are grounded:

$t_{low-high\ (or\ high-low\ )} = \sum_{node\ i} R_{i\_to\_source\ (or\ ground)} C_i$.

Derived Delay Formula for *Diode*:

$$t_{diode} = 0{,}69\left(\frac{C_w}{2}\left(3R_w + 2(2R_{W\_CP} + R_{ON})\right) + k_2 C_{CP}(R_w + 2R_{W\_CP} + R_{ON})\right) \quad (1)$$

Derived Delay Formula for *FET*:

$$t_{FET} = 0{,}69\left(\frac{C_w}{2}(3R_w + 2R_{ON}) + 3C_{CP}(R_w + R_{ON})\right) \quad (2)$$

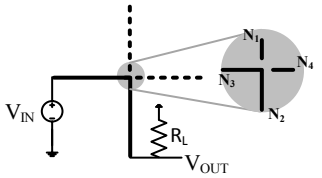
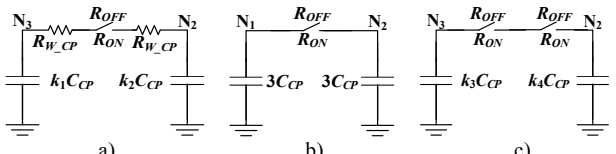


Fig. 6. Test circuit, used in performance model and analysis.



a) b) c)

$k_1 = \left(\frac{R_{W\_CP} + R_{ON}}{2R_{W\_CP} + R_{ON} + R_w + R_L}\right)$	$k_2 = \left(\frac{3R_{W\_CP} + 2R_{ON}}{R_w + R_L}\right)$
$k_3 = \left(\frac{R_{ON}}{2R_{ON} + R_w + R_L}\right)$	$k_4 = \left(\frac{3R_{ON}}{R_w + R_L}\right)$

d)

Fig. 7. Crosspoint modeling of the test circuit for a) diode based, b) FET based, and c) four-terminal switch based. The k_i values are shown in d).

Derived Delay Formula for *four-terminal*:

$$t_{4-term} = 0{,}69\left(\frac{C_w}{2}(3R_w + 2(2R_{ON})) + k_4 C_{CP}(R_w + 2R_{ON})\right) \quad (3)$$

We calculate power consumption as the sum of active and passive power (notice that f can be calculated as $(1/t_{delay})$ in (4). Here, the first and the second terms represent active and passive power consumptions, respectively; C_{total} is the direct sum of all model capacitors; R_{total} is the equivalent resistance between V_{DD} and GND.

$$P = C_{total} {V_{DD}}^2 f + {V_{DD}}^2 / R_{total} \quad (4)$$

The area of a 1×1 crosspoint used in the test circuit can be calculated as (where D and p_w represent wire diameter and pitch size, respectively):

$$Area = (D + p_w)^2 \quad (5)$$

A. Technology Considerations

In this section we thoroughly explain how to find real values of the parameters used in above formulas. For our calculations, we use a minimum wire diameter D of 1nm and a minimum pitch size p_w of 10nm by considering nanowire array technology limits [10]. We also limit ranges for nanowire electric current values between 10uA - 20 uA and a supply voltage V_{DD} between 1V - 5V [21]. Insulator layer between wires is selected as SiO_2 [12]. Minimum value for the layer thickness t_l is selected by assuming that there is no substantial leakage. For SiO_2, at least 1.2 nm thickness is preferred [20]. In this study we use t_l =1.5nm, slightly larger than the minimum.

For capacitor and resistor calculations, we use standard equations $C = \frac{K.\varepsilon.A}{L}$ and $R = \frac{\delta.L}{A}$. For FET and four-terminal switch based arrays. We exploit wire and resistance specifications as well as substrate material types according to [11-12]. Resistance values of *n*-type and *p*-type nanowires with 10nm length and 1nm^2 cross-section area are selected as 10kΩ and 38.1 kΩ, respectively [12]. To achieve 1/10 ratio between wire and crosspoint resistances (R_{ON}), we select 100kΩ and 381kΩ for crosspoint resistance s for *n*-type and *p*-type nanowires, respectively. This satisfies our goal of having electric current values between 10uA and 20uA. By using the standard resistor equation, we can find any desired resistance value with given wire dimensions. Different than the other two counterparts, diode based arrays have a different calculation method. We used doping values from [19] and material constants for silicone to calculate resistance values.

Nanowire capacitors C_w's are composed of parasitic wire, parallel wire, wire-layer, and wire-bulk capacitors. We approximate C_w's with only using parallel plate wire-bulk capacitors since the values of other capacitors are generally negligible. Capacitance between two nanowires in the crossing area is represented by four equal C_{CP} capacitors. One C_{CP} capacitor is a quarter of the total crosspoint capacitance. The total crosspoint capacitor can be directly calculated using the standard capacitor equation and given dimensions. Additionally, for diode based crosspoints we use diffusion capacitance formula $C_{CP\_Diode} = \frac{\mathrm{kSi.e.A}}{\mathrm{w.V_d}} I_D$. Note that the capacitor plate area $A=D^2$ and the distance between plates $L= t_l$.

B. Performance Analysis

It is important to note that resistance and capacitance values of nano-crossbar arrays directly depend on the parameters t_I, D, and p_w. In this section, we analyze the effects of these parameters on power-delay-area performance of the arrays. We use intervals of 1nm-30nm for D and 10nm-90nm for p_w. Additionally we use different fan-out capacitors, 0.1fF to 2fF, to test the integration capability of the arrays. All of the results in this section are obtained using the test circuit comprising a single crosspoint, shown in Fig. 6.

Table 1 summarizes performance characteristics of the three types of nanowire technologies. It shows lower and upper limits for each performance metric for 1nm$\leq D \leq$10nm, 10nm $\leq p_w \leq$ 20nm, t_I=1.5nm, and a fan-out capacitor C_L=0.1fF. Examining the numbers in the table, we see that the diode based array has the best "no-fan-out delay" span, but for "with fan-out" case, all the three technologies have close values. For power consumption, very close results are obtained for all types. Area values are same for all types since we only calculate the unit crosspoint area. Of course, if we implemented Boolean functions or specific benchmark circuits, there would be dramatic differences on the area for these three array types [24]. Although Table 1 offers us valuable information for the performance limits of the arrays, it does not tell us how the parameters D, C_L, and p_w effect each performance metric and how to make performance optimization with the parameters. We explicitly show this for the FET based crosspoints in the following parts.

FET Delay Analysis:

As seen in Fig. 8, increasing wire diameter D or pitch size p_w values make the delay values increase. Increasing D make capacitor values increase and resistor values decrease, and inversely, increasing p_w make capacitor values decrease and resistor values increase. So that delay values always increase, that can be justified using (2). When a fan-out load capacitor C_L is added then (2) becomes:

$$t_{fet} = 0{,}69\left(\frac{C_w}{2}(3R_w + 2R_{ON}) + 3C_{CP}(R_w + R_{ON}) + C_L(2R_w + R_{ON})\right). \quad (6)$$

TABLE I. PERFORMANCE CHARACTERISTICS OF THREE TYPES OF NANOWIRE TECHNOLOGIES USING MAX-MIN VALUES FOR D AND P_W.

Analysis Output	FET	Diode	Four-terminal
Delay (ps)	0.15-0.25	0.013-0.024	0.04-0.16
Delay (ps) with 0.1fF fan-out	20-120	2-15	2-18
Power (uW)	0.02-0.16	0.01-0.25	0.02-0.3
Power 0.1fF fan-out (uW)	2.5-2.6	2.5-2.7	2.5-2.8
Area (nm^2)	200-900	200-900	200-900
Power × Delay (uW × ps)	0.02-0.09	0.02-0.018	0.01-0.6

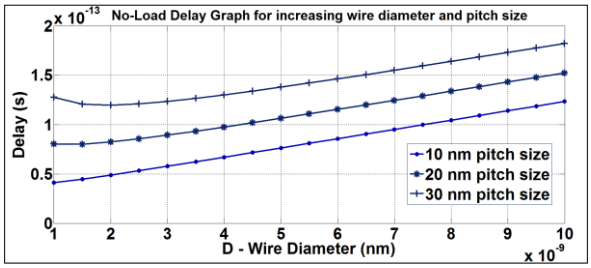


Fig. 8. FET delay for no-load case.

Fig.9 shows results of (6) with C_L=0.1fF. Here, increasing D values make the delay values decrease almost independently with changes in p_w. There are 3 different p_w values selected in the Fig. 9 and corresponding delay values have relatively small differences. This concludes that, considerably larger fan-out capacitors compared to wire/crosspoint capacitors, suppress pitch size effect on the circuit delay. This situation gives us important inferences for the integration of nanowire circuits with the CMOS technology. As clearly seen from Fig. 9, increasing D values are beneficial for the CMOS integration which also slightly increase the area. On other hand, changing p_w values does not give us a considerable benefit for the integration problem, so we can select minimum p_w values to decrease area.

FET Power Analysis:

Power values are calculated using (4). In this equation, f is selected as 1 GHz, which is a satisfactory speed for logic circuits. Also a fan-out load capacitor of 0.1 fF is added. As shown in Fig. 10, D is very dominant over p_w for small D values. Another inference is that using smaller circuits by selecting small D and p_w values results in smaller power consumption.

FET Area Calculations:

Area calculations are straightforward using (5). Here, D and p_w have same linear relationships with the area.

FET Maximum Frequency and Power×Delay Analysis:

Fig. 11 shows maximum achievable frequency levels by considering different D and C_L values; p_w is selected as 10 nm. As seen in the Fig. 11, if the fan-out capacitance gets smaller, effect of D on the maximum frequency increases. Depending on the fan-out capacitance value, maximum frequency can be both negatively and positively correlated with D. For example, consider a 0,001 fF capacitance at the output. Maximum frequency increases up to D = 6 nm and decreases afterward. So we can say that, for this case, maximum frequency could be achieved with selecting 6 nm wire diameter. The power×delay graph is given in Fig. 12. Here, selecting minimum pitch sizes and minimum wire diameters is highly preferable.

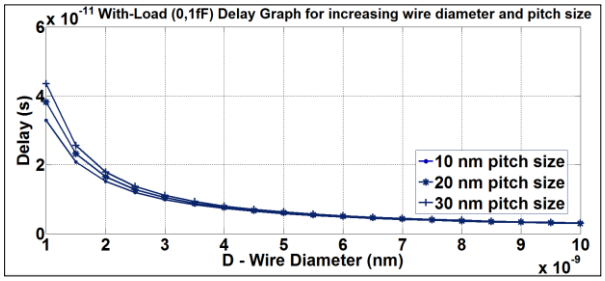


Fig. 9. FET delay with a fan-out capacitance (0.1 fF).

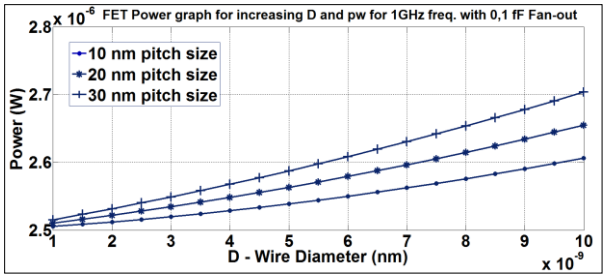


Fig. 10. FET power with 1GHz frequency and a 0.1 fF fan-out capacitance.

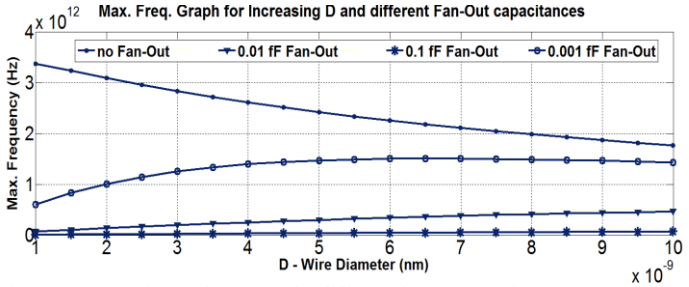


Fig. 11. FET maximum frequency for different fan-out capacitances (10 nm p_w).

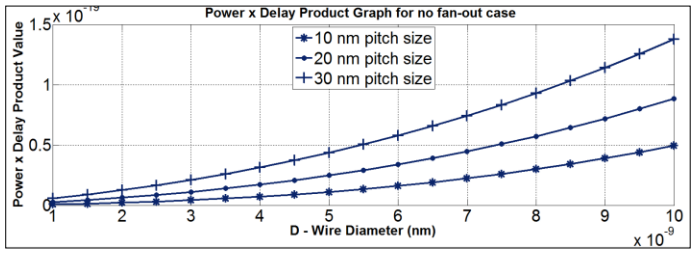


Fig. 12. FET power-delay product for no-load case.

IV. Evaluation of the Proposed Capacitor-Resistor Models Given in Section 2

We evaluate our capacitor-resistor models proposed in Section 2 using a circuit simulation program SPICE. We implement XOR_3 function since it is the fundamental function of full adder circuits (analyzed in the next section, Fig. 13). We consider three cases:

***Case*-1:** $5C_{CP} \cong C_w$ (D=1nm, p_w=10nm),
***Case*-2:** $C_{CP} \cong 2C_w$, by changing D=10nm,
***Case*-3:** Keeping C_{CP} value same as in *Case*-1 and $C_w = 0$ (negligibly small as frequently done for CMOS).

"*Case*-1" is the case with minimum distances. In order to increase the effect of C_{CP} capacitor over C_w, we introduce "*Case*-2" and "*Case*-3" where wire diameter is increased, so C_w becomes negligibly small (let t_{bulk} (bulk thickness) is infinite). Results are shown in Table 2 for worst-case low-to-high propagation delays. As we propose and claim in Section 2, our general model based on physical reasoning, illustrated in Fig. 2 and Fig. 3, is considered error free. We name it "wire-wire" since crosspoint capacitors are put between wires. Additionally, our simplified model named as "wire-ground C_{CP_eqv}=3C_{CP} (and 4C_{CP})", illustrated in Fig. 7b), is considered.

TABLE II. Worst-Case Low-to-High Propagation Delay Analysis Using Different Capacitor-Resistor Models (***Proposed**)

	C_{CP} connection type	Delay (ps)	Error %
***Case*-1**	wire-wire - *	8.31	0
	wire-ground C_{CP_eqv}=2C_{CP}-[10-13]	8.239	0.853
	wire-ground C_{CP_eqv}=3C_{CP} - *	8.266	0.527
	wire-ground C_{CP_eqv}=4C_{CP} - *	8.293	0.200
***Case*-2**	wire-wire - *	153.139	0
	wire-ground C_{CP_eqv}=2C_{CP}-[10-13]	145.958	4.689
	wire-ground C_{CP_eqv}=3C_{CP} - *	148.665	2.921
	wire-ground C_{CP_eqv}=4C_{CP} - *	151.370	1.155
***Case*-3**	wire-wire - *	0.778	0
	wire-ground C_{CP_eqv}=2C_{CP}-[10-13]	0.719	7.633
	wire-ground C_{CP_eqv}=3C_{CP} - *	0.746	4.187
	wire-ground C_{CP_eqv}=4C_{CP} - *	0.773	0.725

We compare our models with the ones used in the literature [10-13]. Examining the numbers in Table 2, we see that the proposed wire-ground model overwhelms the compared models. Note that delay values are not changing linearly since C_ws are dominant and proposed C_{CP} values are only applicable for switching inputs.

Of course, a more rigorous comparison would be made in support of experimental characterizations and tests. This is certainly out of scope of our computational work and hope to open new areas for scientists working on experimental nanoelectronics.

V. Performance Analyses of Logic and Memory Applications

A. Logic Application: 1-Bit Full Adder

A 1-bit full adder is implemented with a FET based nanowire crossbar circuit shown in Fig. 13. A complementary logic is used with *p*-type and *n*-type nanowires (proposed in [8]) on the left and the right parts of the circuit, respectively. The inputs are *A, B*, and *Cin*, and the outputs are *S* and *Cout*.

The adder circuit performance is analyzed using different fan-out load capacitors. Results are given in Table 3 that are obtained using D=5nm, p_w=10nm, and t_i=1.5nm. As seen in Table 3, 1 GHz frequency operation can be achieved with no fan-out, 0.1 fF fan-out, and 0.5 fF fan-out capacitances for this case. When 2 fF fan-out capacitance is added, maximum frequency drops to 0.67GHz, which is much lower than the desired frequency of 1GHz. To fix this problem, when C_L=2fF, we can use larger D or p_w values. When D = 8 nm and p_w = 10 nm, the frequency becomes 1 GHz. On the other hand, using a diameter of 8nm is a certain drawback for the circuit area. Increasing p_w is the other option, but as seen in Fig. 9, p_w has almost no effect on delay in case of having relatively large fan-out capacitors.

B. A Memory Application: 4x4 Nand Based Rom

A typical organization of a nanoarray ROM is given in Fig 14. Here, in middle part, the given inset table is implemented with FET based nanowire arrays using a pseudo-NMOS NAND based memory structure. Decoder and DeMux devices can be also implemented by diode or FET based nanoarrays. For area calculation of the memory, parameters of *n* word lines, *m* bit lines, wire diameter *D,* and pitch size p_w can be used:

$$Area_{ROM} = 2.n.m.(D + p_w)^2. \quad (7)$$

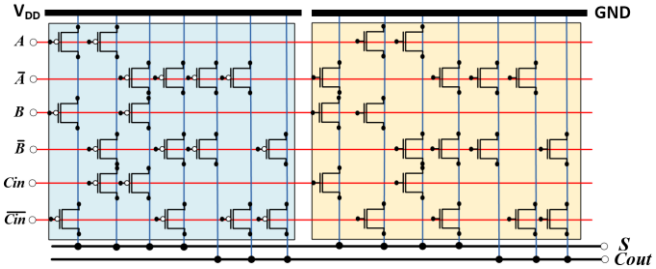


Fig. 13. A FET based nanowire crossbar array implementing a 1-bit full adder.

TABLE III. 1-Bit Full Adder Performance Values

	No fan-out	0,1 fF	0,5 fF	2 fF
High-to-Low Delay (ps)	0.46	15.7	77.1	307
Low-to-High Delay (ps)	1.75	60.1	293	1160
Power (1GHz) (uW)	0.212	2.71	12.7	50.2
Maximum Frequency (GHz)	452	13.1	2.69	0.67<1!

If nanowires on this circuit are considered with a 1 nm diameter, we can estimate a reasonable access time by using the calculations Section 3. There would be 7-10 transistors on the data transit line between S0 or S1 and Z due to modeling of the decoder and the DeMux. Also we can add a 0,1 fF capacitance to the Z node to look for MOS device compatibility of this memory. After modeling RC ladders, the achieved reasonable access time intervals are:

2.7 – 3.2 ps for "*No load on Z*"; and

96 – 108 ps for "*0.1 fF load on Z*".

Note that here we present preliminary results for nanoarray based memory circuits. In future work, we aim to perform a much more detailed analysis considering different memory structures with additional performance metrics.

VI. Conlusion

This study proposes a capacitor-resistor circuit model for the crossbar structured nanoarrays in order to accurately analyze power/delay/area performance characteristics. Although the proposed model is technology independent, we explicitly show its applicability for three different nanoarray technologies where each crosspoint behaves as a diode, a FET, and a four-terminal switch. In order to find related capacitor and resistor values, we investigate upper/lower value limits for technology dependent parameters including doping concentration, nanowire dimensions, pitch sizes, and layer thicknesses. We also use different fan-out capacitors to test the integration capability of these technologies. Comparison between the proposed model and a conventional simple one, which generally uses one/two capacitors for each crosspoint, demonstrates the necessity of using our model in order to accurately calculate power and delay values. In experimental results, we accurately analyze a 1-bit full adder with the proposed capacitor-resistor models. We also make a brief performance analysis of a memory circuit.

As a future work, we plan to construct a more comprehensive circuit model to be integrated to circuit simulation tools. The model will include both memory and arithmetic circuit elements.

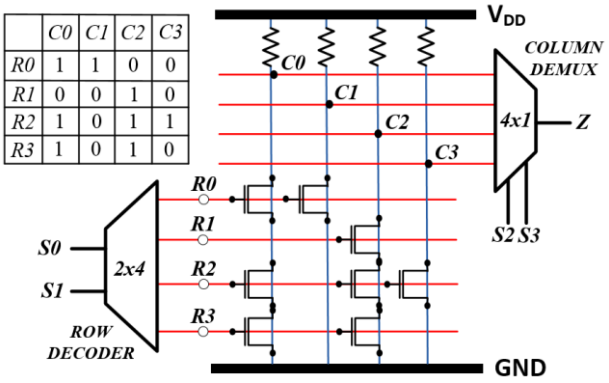


Fig. 14. 4x4 pseudo-NMOS ROM array with row decoder and column DeMux devices. Inset table gives data stored on memory array Z output gives selected data by S0, S1, S2 and S3 access inputs.

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References

[1] "Overall Technology Roadmap Characteristics". International Technology Roadmap for Semiconductors. 2010. Retrieved 2013.

[2] M. Dubash, "Moore's Law is dead, says Gordon Moore." *Techworld* (April 2005).

[3] M. M. Waldrop, "The chips are down for Moore's law." *Nature News* 530.7589 (2016): 144.

[4] K. Ariga et al. "Two-dimensional nanoarchitectonics based on self-assembly." *Advances in colloid and interface science* 154.1 (2010): 20-29.

[5] G. M. Whitesides and B. Grzybowski, "Self-assembly at all scales." *Science* 295.5564 (2002): 2418-2421.

[6] W. Lu and C. M. Lieber. "Nanoelectronics from the bottom up." *Nature materials* 6.11 (2007): 841-850.

[7] Y. Huang et al. "Logic gates and computation from assembled nanowire building blocks." *Science* 294.5545 (2001): 1313-1317.

[8] G. Snider, "Molecular-junction-nanowire-crossbar-based inverter, latch, and flip-flop circuits, and more complex circuits composed, in part, from molecular-junction-nanowire-crossbar-based inverter, latch, and flip-flop circuits." U.S. Patent No. 6,919,740. 19 Jul. 2005

[9] M. Altun and M. D. Riedel. "Logic synthesis for switching lattices." *Computers, IEEE Transactions on* 61.11 (2012): 1588-1600.

[10] M. M. Ziegler et al. "Scalability simulations for nanomemory systems integrated on the molecular scale." *Annals of the New York Academy of Sciences* 1006.1 (2003): 312-330.

[11] M. Dong and L. Zhong. "Logic synthesis with nanowire crossbar: reality check and standard cell-based integration." *Proceedings of the conference on Design, automation and test in Europe. ACM,* 2008.

[12] M. Gholipour and N. Masoumi. "A comparative study of nanowire crossbar and MOSFET logic implementations." *EUROCON-International Conference on Computer as a Tool (EUROCON), IEEE* 2011.

[13] M. Zamani, H. Mirzaei, and M. B. Tahoori. "ILP formulations for variation/defect-tolerant logic mapping on crossbar nano-architectures." *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 9.3 (2013): 21.

[14] Y. Xu, N. Matsumoto, Q. Wu, Y. Shimatani and H. Kawata, "Site-specific nanopatterning of functional metallic and molecular arbitrary features in nanofluidic channels." *Lab on a Chip* 15.9 (2015): 1989-1993.

[15] KH. Kim et al. "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications." *Nano letters* 12.1 (2011): 389-395.

[16] D. B. Strukov and R. S. Williams. "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays." *Proceedings of the National Academy of Sciences* 106.48 (2009): 20155-20158.

[17] W. Shim, J. Yao, and C. M. Lieber. "Programmable resistive-switch nanowire transistor logic circuits." *Nano letters* 14.9 (2014): 5430-5436.

[18] M. Haselman and S. Hauck. "The future of integrated circuits: A survey of nanoelectronics." *Proceedings of the IEEE* 98.1 (2010): 11-38.

[19] S. C. Goldstein and M. Budiu. "Nanofabrics: Spatial computing using molecular electronics." *ACM SIGARCH Computer Architecture News* 29.2 (2001): 178-191.

[20] G. Timp et al. "The relentless march of the MOSFET gate oxide thickness to zero." *Microelectronics Reliability* 40.4 (2000): 557-562.

[21] W. Lu, P. Xie and C. M. Lieber. "Nanowire transistor performance limits and applications." *Electron Devices, IEEE Transactions on* 55.11 (2008): 2859-2876.

[22] W. N. HE. *Cmos Vlsi Design: A Circuits and Systems Perspective, 3/E*. Pearson Education India, 2006.

[23] J. M. Miller. *Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit*. Vol. 351. Government Printing Office, 1919.

[24] M. C. Morgul, and M. Altun. "Synthesis and optimization of switching nanoarrays." *Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2015 IEEE 18th International Symposium on. IEEE*, 2015.