Student Name: Instructor: Mustafa Altun

Student ID:

BLG231E Digital Circuits Homework 1

Deadline: 21/10/2016 (before 9:30)

1. CONVERSION BETWEEN NUMBER REPRESENTATIONS

Perform the following number conversions:

- a) Binary (100111.10111)₂ to decimal, octal and hexadecimal.
- **b)** Octal (72.6)₈ to decimal, binary and hexadecimal.
- c) Hexadecimal (C3.AD5)₁₆ to decimal, binary and octal.

2. SIMPLIFIED SUM OF PRODUCT (SOP) EXPRESSIONS

Express the following Boolean functions in SOP forms with using minimum number literals. Write down the total **number of literals** for your simplified expressions (for example, $x_1\overline{x_2}x_3 + x_1\overline{x_3}$ has 5 literals).

$$\mathbf{a}) \ f_1 = \ \overline{x_1 x_2 + x_2 x_3 + x_3 x_4}$$

b)
$$f_2 = \overline{x_1} x_2 x_3 + x_1 x_4$$

c)
$$f_3 = \overline{x_1}\overline{x_2}x_3 + x_1\overline{x_4} + x_2x_3\overline{x_4}$$

b)
$$f_2 = \frac{\overline{x_1}x_2x_3 + x_1x_4}{\overline{x_1}\overline{x_2}x_3 + x_1\overline{x_4} + x_2x_3\overline{x_4}}$$

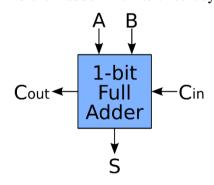
c) $f_3 = \frac{x_1\overline{x_2}x_3 + x_1\overline{x_4} + x_2x_3\overline{x_4}}{\overline{x_1}x_2\overline{x_3} + x_1\overline{x_2}x_3 + \overline{x_1}x_2x_3 + \overline{x_1}\overline{x_2}\overline{x_3}}$

3. DESIGNING A 4-INPUT & 1-OUTPUT CIRCUIT

Consider a circuit with 4 inputs and 1 output such that a transition (0-to-1 or 1-to-0) in one of the inputs always results in a transition at the output (0-to-1 or 1-to-0). Derive the truth table of this circuit.

4. DESIGNING A 1-BIT FULL ADDER

Consider a 1-bit full adder with its circuit symbol and truth table shown below.



<u>Inputs</u> A B Cin	Outputs Cout S
0 0 0	0 0
0 0 1	0 1
0 1 0	0 1
0 1 1	1 0
100	0 1
101	1 0
1 1 0	1 0
1 1 1	1 1

- a) Derive Boolean functions of the outputs in terms of the inputs in both SOP and POS forms. There should be total of 4 expressions.
- b) Implement the adder by only using NAND-2 gates. In your implementation, you need to use the expressions derived in a). Minimize the number of NAND-2 gates in your design.
- c) Implement the adder by only using NOR-2 gates. In your implementation, you need to use the expressions derived in a). Minimize the number of NOR-2 gates in your design.

Grading: 1a)3%, 1b)3%, 1c)3%, 1d)3% 2a)7%, 2b)7%, 2c)7%, 2d)7% 3)15% 4a)15%, 4b)15%, 4c)15%

Note: Return a hard-copy of your homework.