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BLG231E Digital Circuits
FINAL

Duration: 120 Minutes
Grading: 1) 20%, 2) 15%, 3) 25%, 4) 40%
Exam is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

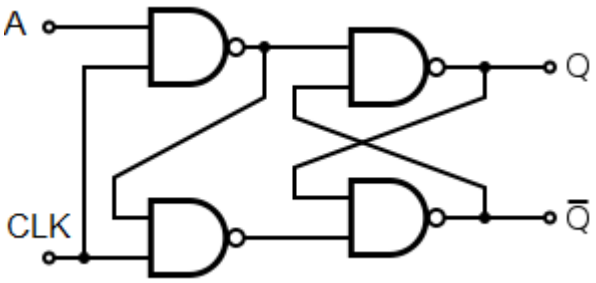
1) Consider a 6-variable Boolean function $f = f_1(x_1, x_2, x_3, x_4) \cdot f_2(x_4, x_5, x_6)$ where $f_1 = \prod(1,2,3,5,7,12,14)$ and $f_2 = \prod(3,4,5,6,7)$. Obtain a minimal product-of-sums (POS) expression for f.

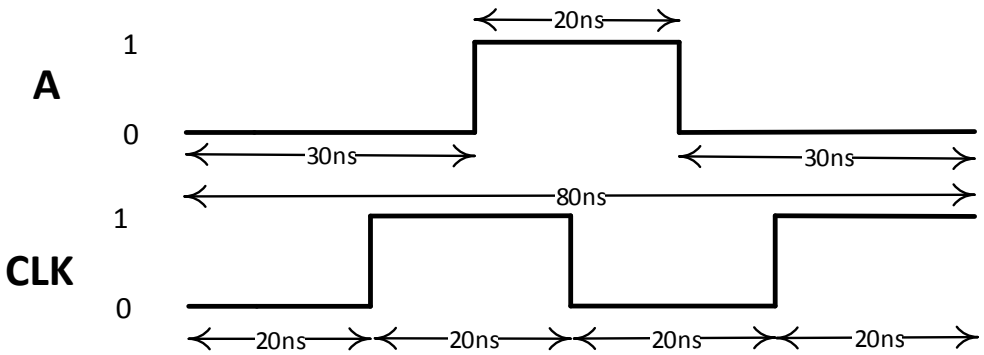
2) Implement a 4-variable Boolean function $f(x_1, x_2, x_3, x_4) = \sum(2,4,5,7,8,9,11,13,15)$ using **a single 4-to-1 multiplexer** and minimal number of **two-input NAND gates.** Use x_1 and x_2 as select input lines in the multiplexer. Use only variables x_1, x_2, x_3, x_4 as inputs (**not their negated forms)**.

3) Consider a flip-flop consisting of four NAND gates, shown below. Suppose that each of the NAND gates has a delay of **2ns**. Suppose that initial values of Q and Q' are 0 and 1, respectively.

a) Obtain **a minimal sum-of-products (SOP) expression for Q** in terms of previous Q, and inputs A and CLK.

b) Sketch the **waveforms at the outputs Q and Q'** if the input signals A and CLK shown below are applied.





4) Consider a **Mealy** machine based sequential circuit having one input **X** and one output **Z**. The output Z will be 0 except the input sequence **1101** are the last 4 inputs received on X. The circuit has 7 states defined as follows:

Input Sequence	**State**
……...00	A
……...11	B
…….001	C
…….010	D
…….110	E
……0101	F
……1101	G

a) Obtain the state table and perform **state reduction**. After state reduction how many states remain?

b) Draw the **state diagram** having the reduced states.

c) Start designing the circuit with assigning 0's and 1's to the reduced states. Your design will be based on D-flip-flops. Derive minimal sum-of-products (SOP) Boolean expressions for the next states and the output in terms of the input and the current states.

d) Draw the circuit using minimal number of **D-flip-flops**, and **AND**, **OR**, and **NOT gates.**

EXTRA PAGE FOR SOLUTIONS