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BLG231E Digital Circuits
MIDTERM II

Duration: 120 Minutes
Grading: 1) 20%, 2) 15%, 3) 35%, 4) 30%
Exam is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

1) Consider Boolean functions $f_1(x_1, x_2, x_3) = \sum(0,1,3,5,6,7)$ and $f_2(x_4, x_5, x_6) = \sum(2,3,4,5,6,7)$. Implement $f = f_1 + f_2$ using **two 3-to-8 decoders** and minimal number of **two-input NOR gates.**

2) Consider a comparator circuit that compares two binary inputs, A and B, and generates a binary output Y, such that Y=1 if and only if these inputs are equal (i.e. A=B).

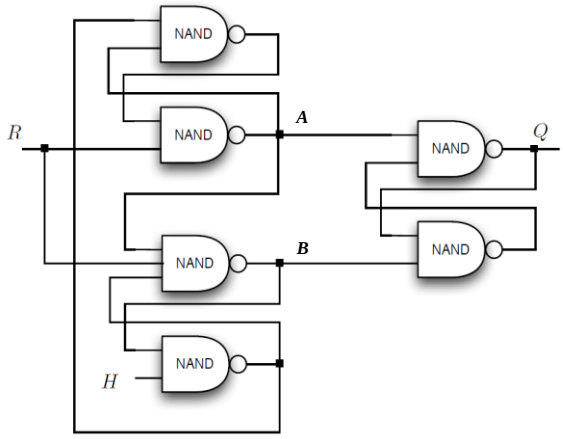
a) Implement a 1-bit comparator using **a single 4-to-1 multiplexer**.

- A and B are 1-bit numbers that results in 2 binary inputs and an output Y.

b) Implement a 4-bit comparator using **four 4-to-1 multiplexers and a single AND gate**.

- A and B are 4-bit numbers A = A3 A2 A1 A0 and B = B3 B2 B1 B0 that results in 8 binary inputs and an output Y.

3) Consider a sequential circuit shown below.



R	H	current Q	new Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

a) Fill out the above table by **inserting new *Q* values**. If **new *Q* values** cannot be precisely determined as logic 0 or logic 1, then express them using **current *A* and *B* values.**

b) Find sum-of-products (SOP) expressions of **new *Q*** in terms of ***R***, ***H***, **current *Q***, **current *A***, and **current *B***.

4) Consider a flip-flop consisting of one inverter, one XOR gate, and four NAND gates, shown below. Suppose that the inverter has a delay of **1ns;** each of the NAND gates has a delay of **3ns;** the XOR gate has a delay of **5ns** . Sketch the **waveforms at the outputs Q and Q'** if the input signals A and CLK shown below are applied. Suppose that initial values of Q and Q' are 0 and 1, respectively.