

BLG231E Digital Circuits

Homework 2

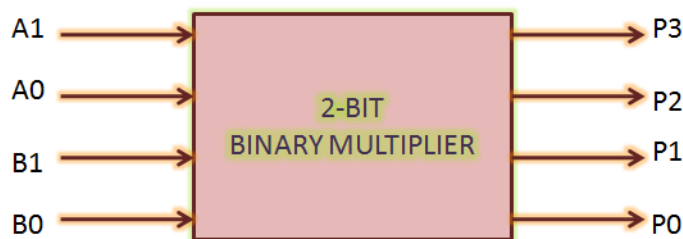
Deadline: 2/12/2016 (before 9:30)

1. LOGIC DESIGN WITH DECODERS AND MULTIPLEXERS

- a) Implement $f(x_1, x_2, x_3) = \prod (0,1,3,6,7)$ by using a single 3-to-8 decoder and minimum number of NAND-2 gates.
- b) Implement $f(x_1, x_2, x_3, x_4) = \sum (3,5,6,7,10,11,12,13)$ by using a single 4-to-1 multiplexer and minimum number of NAND-2 gates.
- c) Implement $f(x_1, x_2, x_3, x_4) = \sum (0,1,4,7,10,13,15)$ by using a single 8-to-1 multiplexer and minimum number of NAND-2 gates.
- d) Implement a 16-to-1 multiplexer by using 4-to-1 multiplexers.

2. DESIGNING A 2-BIT BY 2-BIT MULTIPLIER

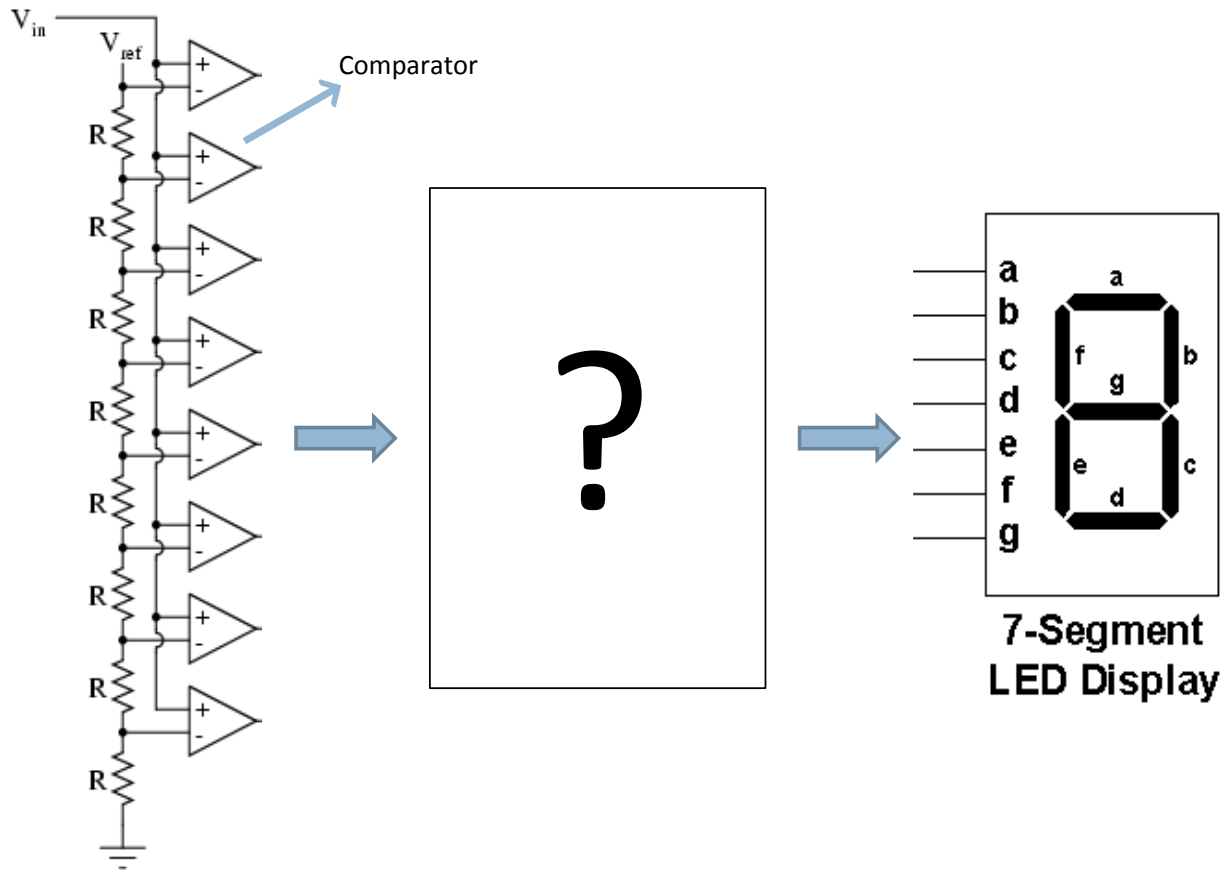
Consider a 2-bit by 2-bit multiplier with its circuit symbol shown below.



- a) Derive a truth table (with 16 rows) for the outputs P0, P1, P2, P3 in terms of the inputs A0, A1, B0, B1. Each row of the table represents a different input assignment. For example, if input binary numbers 11 and 10 are multiplied then the output binary number should be 0110 meaning that A0=1, A1=1, B0=0, B1=1, P0=0, P1=1, P2=1, P3=0 for the corresponding row.
- b) Implement the multiplier by only using **2-to-4 decoders** and **2-to-1 multiplexers**. Suppose that each decoder has a cost of **2** and each multiplexer has a cost of **1**. Minimize the total cost.

3. DESIGN OF AN ANALOG TO DIGITAL CONVERTER

Consider a circuit structure shown below. Suppose that $V_{ref}=8V$. A comparator has an output of logic 1 if the voltage level on its positive input is larger than the voltage level on its negative input. For example, $V_{in}=5.2V$ results in 0, 0, 0, 1, 1, 1, 1, 1 outputs from top to bottom. Design the circuit block such that, if $V_{in} > 8V$, the display shows “8”; if $8V > V_{in} > 7V$, the display shows “7”;.....; if $2V > V_{in} > 1V$, the display shows “1”. Use a **priority encoder**, a **decoder**, and **OR** gates.



Grading: 1)30%, 2)30%, 3)40%

Note: Return a hard-copy of your homework; you can put your homework under my door.